CMOS Image Sensors and 3D Integration

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CMOS Image Sensors and 3D Integration

Agenda

• CIS Market
• *Confirmation* that 3D production has begun
• *Clarification* of 3D development trends and topics
• CIS 3D Drivers & Considerations
• Closing Thoughts
• Q&A
Growing Addressable Market

1. CCD/CMOS Area Sensor Market Trend (Excluding sensor shipments for whitebox and gray camera phone markets)

CCD/CMOS Area Image Sensor Market

* Above data does not include CMOS sensors for whitebox and gray camera phones and optical Mice use

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CIS Applications/Segments

- Mobile
- DSLR / DSC / DVC
- PC & V-Conf
- Gaming
- Auto
- Security
- Scanning
- Other

- IPTV
- Monitors
- Cell Phones
- Notebook
- Tablet
- Telepresence
- Video Phone
- High Speed Digital Video
- Machine Vision
- Surveillance
- Medical
- Gaming
- Digital Still Cameras
- DSLR
- PC

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Confirmation that 3D production has begun
Clarification of 3D development trends and topics

- 200mm (in production now)
  - Via-Last interconnect technologies and considerations in maximizing gross die per wafer

<table>
<thead>
<tr>
<th>Interconnect</th>
<th>Vertical Via</th>
<th>Tapered Via (MVP)</th>
<th>T-Contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scribe Width</td>
<td>&gt;= 80um</td>
<td>&gt;= 80um</td>
<td>&gt;= 160um</td>
</tr>
<tr>
<td>Min. Pad Pitch</td>
<td>100um</td>
<td>130um</td>
<td>200um</td>
</tr>
<tr>
<td>GDPW</td>
<td>100%</td>
<td>100%</td>
<td>96%</td>
</tr>
</tbody>
</table>

Baseline for comparison purposes ~ Equivalent GDPW ~<4% less GDPW
Clarification of 3D development trends and topics

- BSI (Backside Illumination)
  - Improved low light sensitivity as pixel size decreases

- High Dynamic Range
  - Clarity across a variety of lighting levels

- ICP (Imaging Co-Processor)
  - An ISP with increasing functionality

Highly--integrated

FSI BSI

(embedded ISP)

Tuned solution: high performance and unique features
CIS 3D Drivers & Considerations

• 3D Single component solutions
  ‣ Cost (die size, GDPW, yield dependencies)
  ‣ Form Factor (x-y, sensor array to BGA alignment)
  ‣ Yield (glass over sensor protects the array from particle contamination)

• 3D Stack solutions
  ‣ Process optimization for the Sensor and ICP (cost and performance)
    • Sensor process specific to sensor, logic process specific to digital
    • More functions, faster speed, lower power
  ‣ Form Factor (x-y)
  ‣ New/different product development model
    • Late-binding, customization may be possible
    • Separate pieces may be easier to engineer/implement

• Challenges
  ‣ Cost, Performance, and/or Form Factor advantages must be compelling enough to drive adoption
  ‣ Supply Chain is still fragmented and/or lacking in capability
  ‣ BSI presents a unique challenge if Via-First/Middle technology is a consideration
CIS 3D Drivers & Considerations

TSV formation (where in the process?)

- **Via-First/Middle**
  - Predetermines final product at Foundry

- **Via-Last**
  - Enables 3D as a packaging solution independent of Foundry

Do I make the Engineers happy?

Do I make the Supply Chain team happy?

Does either approach make the business “happy”?
CIS 3D Drivers & Considerations

The answer.....

• Keep the business “happy” by leveraging the advantages of each

• Via-First/Mid
  ‣ Allows for higher density interconnect schemes (1000’s+)

• Via-Last
  ‣ Allows for flexibility in supply chain management (delays timing of when Si is “committed” to a specific product)
    • Example: Sensor or ICP can complete full Front End flow w/o disruption and then be staged for single component or stack solutions at start of Back End flow

• 300mm offers a clean slate
  ‣ Approaches are being vetted, specifically around the TSV technology deployed

• Technology platforms are available
  ‣ Challenge is putting the building blocks together to enable the end solution
CIS 3D Considerations - Stacking

Via-First/Middle

• Enables Wafer-to-Wafer approach

Via-Last

• Enables Die-to-Wafer approach
CIS 3D Drivers & Considerations

Stacked Solutions: Wafer-to-Wafer / Die-to-Wafer

**Sensor/Coprocessor Sq. Area**

<table>
<thead>
<tr>
<th>Ratio (Sensor to Coprocessor)</th>
<th>Relative die size (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>1.1</td>
</tr>
<tr>
<td>1.3</td>
<td>1.4</td>
</tr>
<tr>
<td>1.6</td>
<td>1.7</td>
</tr>
<tr>
<td>1.9</td>
<td>2.1</td>
</tr>
<tr>
<td>2.3</td>
<td>2.6</td>
</tr>
<tr>
<td>2.9</td>
<td>3.2</td>
</tr>
<tr>
<td>3.6</td>
<td>3.9</td>
</tr>
</tbody>
</table>

**Sensor/Coprocessor Yield**

<table>
<thead>
<tr>
<th>Ratio (Sensor to Coprocessor)</th>
<th>Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.89</td>
<td>70%</td>
</tr>
<tr>
<td>0.90</td>
<td>75%</td>
</tr>
<tr>
<td>0.91</td>
<td>80%</td>
</tr>
<tr>
<td>0.92</td>
<td>85%</td>
</tr>
<tr>
<td>0.94</td>
<td>90%</td>
</tr>
<tr>
<td>0.95</td>
<td>95%</td>
</tr>
<tr>
<td>0.96</td>
<td>100%</td>
</tr>
<tr>
<td>0.97</td>
<td>100%</td>
</tr>
<tr>
<td>0.99</td>
<td>100%</td>
</tr>
<tr>
<td>1.00</td>
<td>100%</td>
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Die-to-Wafer

Wafer-to-Wafer

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Closing Thoughts

• The challenges and opportunities in the CIS industry continue to evolve and more than ever packaging is at the crossroads of enabling or hindering Si solutions.

• To ensure that packaging is an enabling technology it will take a concerted effort on the part of the 3D CIS Supply Chain to make it a reality.

• The entity who acts first in successfully consolidating these activities will achieve a critical mass which will set the standard.