Enabling Metal Deposition Technology for High-κ Metal Gate Integration

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Introduction

In the past years, high-k gate dielectric has come to the real chip manufacturing world. Metal gate is required for hafnium based high-k dielectric integration. Gate first flow requires high thermal budget after metal gate process, which limits work function tuning by metal gate material change. One of the most promising approaches is the combination of one mid gap metal gate with two metal oxide capping layers to obtain the required work function for both PMOS and NMOS [1-4]. In this approach, metal gate process should cause no degradation to the gate dielectric and the interface, no effect on equivalent oxide thickness (EOT), and provide highly uniform and repeatable thin film deposition. On the other hand, PVD is known to be one of the most robust technologies for metallization. However, the conventional PVD chamber was designed to deposit relatively thick film with good step coverage which usually requires high plasma density. Hence, a new refined PVD based process was required for metal gate disposition for high-k integration.

The purpose of this study is to develop low damage, production-worthy metal gate process using RF-PVD technology, which has already successfully demonstrated the production worthy performance for metal oxide capping layer deposition for effective work function tuning [5]. In this study, titanium nitride was mainly investigated as mid-gap metal for gate first flow with metal oxide capping layer for effective band-edge work function.

Experimental

MOSCAP devices were fabricated with the process flow shown in Figure 1 on 300mm p-type Si wafers. After gate dielectric stack growth, 5-10nm metal gate was deposited in various conditions. High temperature anneal by RTP was performed after poly deposition to simulate high thermal budget of gate first process. HFCV and IV test were performed for the MOSCAP samples.

Results and Discussion

Prior to MOSCAP test, plasma induced damage was investigated using SPIIDER wafers [6]. It showed no degradation in gate leakage current after RF-PVD TiN process, which confirmed no significant plasma induced damage by RF-PVD.

After optimizing TiN blanket film uniformity, the process was further optimized to improve electrical parameter uniformity with MOSCAP. Figure 2 shows flat band voltage uniformity with different RF-PVD TiN process conditions on SiO2 gate. Good within-wafer uniformity of Vfb was achieved by process condition “C”, less than 2%, 1σ, by optimizing process parameters such as gas flow rate and RF power. Next, the impact of metal gate on EOT was investigated with various process conditions using HfO2 gate stack. Figure 3 shows the effect of TiN composition on the EOT. It was found that high nitrogen conditions caused higher capacitance equivalent thickness (CET) than lower N concentration after high thermal budget. TiN composition also affected the flat band voltage. Higher nitrogen showed higher Vfb. RF-PVD metal gate process was optimized for minimal impact on the high-k dielectric and the interfaces as well as for good within wafer uniformity of electrical parameters. Figure 4 shows the leakage current performance with TiN metal gate deposited by three different technologies: 1) conventional PVD; 2) atomic layer deposition (ALD); 3) RF-PVD. RF-PVD showed the lowest gate leakage at thin CET compared to the other technologies. RF-PVD also showed low interface damage comparable to ALD-TiN (Table 1), which is lower than the conventional PVD process.

Moreover, the combination of the optimized metal gate TiN and LaOx capping layer achieved flat band voltage shift close to NMOS target work function with no CET change (Fig. 5). RF-PVD TiN also demonstrated superior uniformity (Fig. 6) and particle performance during the extended run.

Conclusion

Thus, RF-PVD is a production worthy technology of metal gate deposition and the combination of RF-PVD metal gate and capping layer provides a critical solution for gate-first MOSFET gate integration.

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I. Introduction

Metal oxide deposition

Higher ALD

Metal oxide cap

Metal Gate: RF-PVD TiN

doped poly + RTP (1080°C)

Pre-clean + PVD+ TiN

Metal Gate: MOSCAP Pattern

Electrical Test

Figure 1. MOSCAP process flow and x-TEM of high-k and metal gate

<table>
<thead>
<tr>
<th>TiN Process</th>
<th>Gate Dielectric</th>
<th>( D_s ) ( [\text{cm}^{-2}\cdot\text{V}^{-1}] )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional PVD</td>
<td>SiO(_2)+HfO(_2) (2nm)</td>
<td>( 1.3 \times 10^{12} )</td>
</tr>
<tr>
<td>RF-PVD</td>
<td>SiO(_2)+HfO(_2) (2nm)</td>
<td>( 2.2 \times 10^{12} )</td>
</tr>
<tr>
<td>ALD</td>
<td>SiO(_2)+HfO(_2) (2nm)</td>
<td>( 2.1 \times 10^{12} )</td>
</tr>
<tr>
<td>Poly Ref.</td>
<td>SiO(_2) only (7nm)</td>
<td>( 5 \times 10^{11} )</td>
</tr>
</tbody>
</table>

Table 1. Interface state density with various TiN by the conductance method

Figure 2. Probability plots of flat band voltage with TiN metal gate on SiO\(_2\). 20 sites were tested within a wafer as shown in the map. The uniformity was optimized by changing process parameters such as gas flow rate and RF power. Process “C” shows tight distribution of \( V_{FB} \) across the wafer.

Figure 3. High N concentration in TiN shows higher CET in various RF-PVD process conditions. N-rich TiN also provided higher flat band voltage on SiO\(_2\)/HfO\(_2\) gate stack.

Figure 4. Jc-CET trends with TiN metal gate deposited different hardware. RF-PVD TiN shows better scalability than conventional PVD or ALD.

Figure 5. Effect of metal gate TiN condition and LaOx capping layer addition on CET and flat band voltage.

Figure 6. RF-PVD TiN extended run thickness uniformity.