CVD Co Capping Layers for Cu/Low-k Interconnects: Cu EM enhancement vs. Co thickness

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***Abstract*—Co films with various thicknesses were selectively deposited as Cu capping layers by chemical vapor deposition technique. Selectivity of the Co deposition between Cu and dielectric surfaces was improved by both raising the deposition pressure and adopting a pre-clean process prior to the Co deposition. Degree of electromigration resistance enhancement was observed to be dependent on the deposited Co thickness. Compared to the no-Co control, significant EM lifetime enhancement was observed when the Co cap is thicker than 6nm.**

I. Introduction

As Cu interconnect feature sizes continue to shrink in nanoelectronic applications, electromigration (EM) lifetimes drop rapidly due to a scaling phenomenon and reduction of critical void size for the failure. Although the fast diffusion path in the Cu interconnects varies depending on the overall integration scheme and materials used for chip fabrication, it has been observed that as Cu atoms transported along the metal/post planarized dielectric cap interface play a critical role on the EM lifetime projection. The interface between the dielectric capping layer and the Cu line represents a location that is susceptible to EM -induced mass flow [1], and this fast Cu diffusion path can be effectively suppressed by capping the Cu line with a metal capping layer [2]. While various alternate metal capping approaches have been proposed to reduce Cu transport and void growth [2-7], virtually all involve a tradeoff between EM improvement and Cu resistivity increase. Additional liabilities may include undesirable line-to-line leakages and capacitance increases [3, 7]. For instance, the implementation of a selective metal cap via electroless deposition is challenged by difficulty in preventing contamination of the dielectric surface from the plating bath. In addition to leakage, yield degradation, and other reliability related issues, a contaminated dielectric surface could also impact overall interconnect capacitance. This electroless plating approach also adds processing steps, for example pre- and post-cleans, and increases wafer cost.

It has been reported that neither Co nor Ru is a good oxidation barrier [8]. A passivated Cu interconnect surface with either the material could get oxidized after exposing to the atmosphere. A controlled process queue time between the metallic capping layer deposition and an oxidation barrier layer deposition is therefore critical to prevent oxidation of the Cu surface. Compared to a thin layer, a thicker metallic capping layer is also preferred to avoid the Cu surface oxidation during the air break.

II. Device Fabrication

In this study, patterned wafers were fabricated using 32 nm complementary metal oxide semiconductor (CMOS) test vehicles consisting of one single damascene Cu M1 and two dual damascene Cu Mx levels in a porous organosilicate-glass (OSG) dielectric, and one Al termination level in FTEOS dielectric for electrical parametric check of the process selectivity and for electromigration resistance evaluation of the resulted Co/Cu interface. After dielectric patterning, Cu diffusion barrier was deposited in a 300mm deposition system integrated with degas, Ar+ sputter, PVD Ta(N), and PVD Cu seed deposition chambers. Conventional Cu electroplating and chemical-mechanical polishing (CMP) were performed on the patterned wafers. Selective CVD Co cap layers were then deposited on the exposed Cu interconnects, followed by a standard $SiC_xN_yH_z$ dielectric cap layer deposition, and then subsequent wiring levels were built.

Co containing carbonyl precursor was used in the current study for chemical vapor deposition of Co. The Co carbonyl precursor is stored in the ampoule in an atmosphere comprising helium inert gas. A degas process at 300°C in Ar was performed for 80 sec before the Co deposition process. Selectivity of the deposited Co between the Cu and the dielectric surfaces was compared among various processes, including two pre-clean processes and two Co deposition pressures. The pre-clean process was performed prior to the selective CVD Co deposition and was intent on removing native oxide from the Cu surface and forming a hydrophobic dielectric surface.

III. Characterization Results

For electrical and reliability evaluations, patterned wafers were fabricated using 32nm CMOS test vehicles. After Cu M2 CMP, some wafers were selectively capped with CVD Co, then all were capped with blanket $SiC_xN_yH_z$ dielectric. Figure 1 shows line-to-line leakage measurements from a baseline selective CVD Co metal cap process (reactor condition: 200°C, 10 Torr) without any pre-clean step prior to the Co deposition. This test was carried out in a Cu comb- serpentine structure with ~50 nm wide lines and spaces. The leakage currents and yields depend on the deposited Co cap thickness,

and show higher leakages and lower yields with increasing the CVD Co thickness. Compared to the no-Co control, no leakage current increase or yield degradation is observed up to 30A. However, complete selectivity is not observed and the leakage yield degrades when the deposited Co thickness is up to 45A, which is an indication of Co nucleation on the intra-line dielectric surface. The selectivity of CVD Co process is completely lost and results in <50% leakage yield when the deposited Co thickness is up 90A.

In order to enhance the Co deposition selectivity, a higher Co deposition pressure process at 20 Torr, and two pre-clean processes were checked and compared with the CVD Co baseline control. Figure 2 shows line-to-line leakage measurements from the same test macro used in the previous study. The data shows an obvious enhancement of the Co deposition selectivity from the high pressure process (20 Torr), and indicates no leakage current increase or yield degradation up to 90A. Further selectivity enhancement of the CVD Co process is observed from both the pre-clean processes as shown in Figure 2. As compared to the baseline control processed at 10 Torr, adopting pre-clean I prior to the CVD Co process results in no leakage current increase and no yield degradation up to 60A. However, a small amount of leakage yield degradation is observed when the deposited Co thickness is up to 9nm. Complete Co selectivity from the low pressure deposition process (10 Torr) is demonstrated up to 9nm only from pre-clean II process. Figure 2 also shows no negative impact on leakage yields from both the pre-clean splits when a high pressure condition (20 Torr) is applied during the Co deposition process.

In order to confirm the deposited Co thickness on the Cu surface, transmission electron microscope (TEM) analysis was performed on two patterned samples with target Co thickness of 6nm and 9nm.. Since Co has virtually no atomic number contrast relative to Cu and is very difficult to visualize, elemental mapping analyses by both energy dispersive X-ray (EDX) and electron energy-loss spectroscopic (EELS) are performed to measure and visualize the Co capping layer at the top Cu surface. For the 6nm target-thickness sample, the measured Co thickness from EDX and EELS is 6.2nm and 5.7nm, respectively, Figures 3. The measured thicknesses are based on full with at half maximum of detected Co signal. Figure 4 shows EDX mapping results of detected Ta at the sidewall of the Cu line (a), Cu (b), and Co at the top surface of the Cu line (c). A color overlay (Cu-orange, Ta-pink, Co-yellow), Figure 4 (d), clearly shows the Co extending over the entire $SiC_xN_yH_z$/Cu interface. The results also show no detectable nucleation of Co on the exposed dielectric. The same TEM analysis indicated above was repeated at the 9nm target-thickness sample. The results are shown in Figures 5 and 6. Again the measured Co thicknesses are within a good range as compared to the target thickness. Also, no detectable nucleation of Co is observed on the exposed dielectric.

The via and line resistance measurements from the same wafers are shown in Figures 7(a) and (b). Comparable line resistances are observed between the control and experimental splits, and no line resistance impacts from the Co capping process is confirmed. The measured via resistance values increase with the deposited Co thickness as shown in Figure 7(b). Compared to the no-Co control, the resistance increase is neglectable when the deposited Co thickness is <6nm. About 2x resistance increase is observed from the 7.5nm Co process as compared to the no-Co control.

In order to confirm the Co/Cu interfacial property for use in the Cu interconnects, an EM evaluation was checked in a structure consisting of Cu contact plugs and 200 μm long, ~55nm wide Cu line located above. The testing was performed under a constant current density of 25 mA/μm2 at 300°C. Failure was defined as a 10% resistance change, and the failure distribution was assumed to be lognormal. Figure 8 shows representative failure distributions for the control and Co capped samples. The data shows EM resistance enhancements for the Co-capped Cu interconnects, and indicates degree of EM resistance enhancement dependency on the deposited Co thickness. Compared to the no-Co control, 2~3x longer lifetime is observed from the 1.5nm and 3nm Co samples. Further electromigration lifetime enhancement (>30x) is observed when the Co thickness is >6nm.

IV. CONCLUSION

In summary, Co films were selectively deposited as Cu capping layers by CVD. The deposition process at 20 Torr results in better selectivity between Cu and dielectric surfaces than 10 Torr. Further selectivity enhancement is demonstrated by adopting a pre-clean process prior to the Co deposition. Electromigration evaluation results show degree of EM resistance enhancement dependency on the deposited Co thickness. Compared to the no-Co control, significant EM lifetime enhancement is observed when the Co thickness is >6nm.

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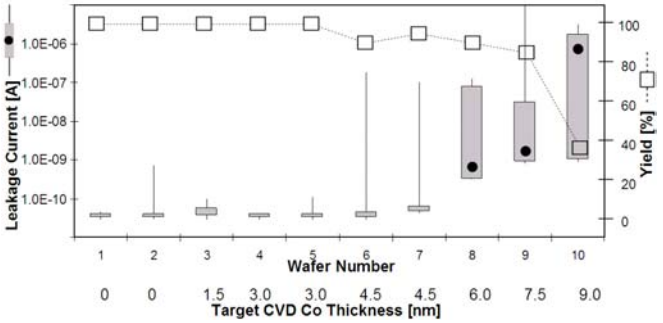

FIG. 1: Leakage measurements from 10 Torr CVD Co process.

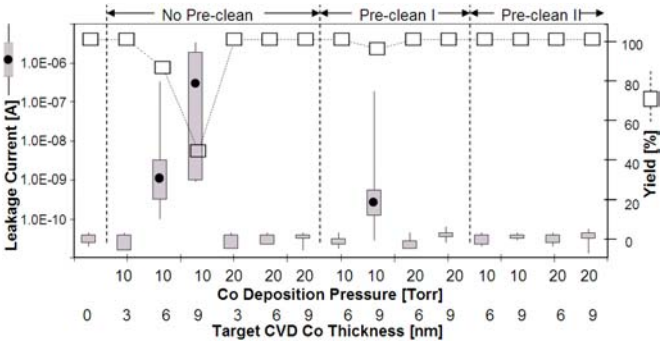

FIG. 2: Leakage measurements.

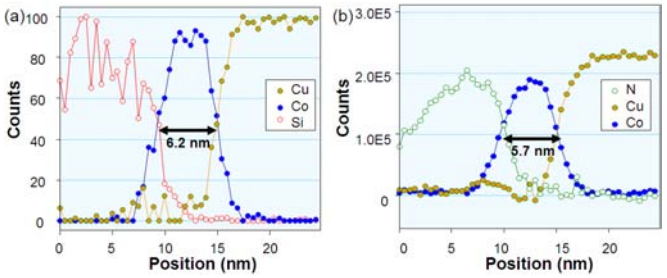

FIG. 3: Co cap thickness measurements from (a) EDX, and (b) EELS. The target thickness is 6nm.

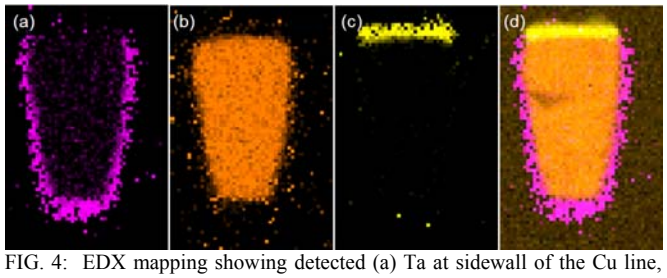

FIG. 4: EDX mapping showing detected (a) Ta at sidewall of the Cu line, (b) Cu, and (c) Co at top surface of the Cu line. (d) Color overlay showing Co covering the Cu surface.

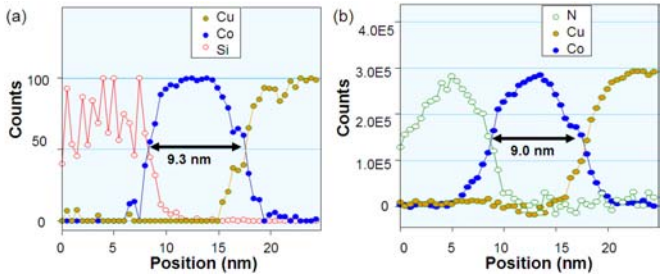

FIG. 5: Co cap thickness measurements from (a) EDX, and (b) EELS. The target thickness is 9nm.

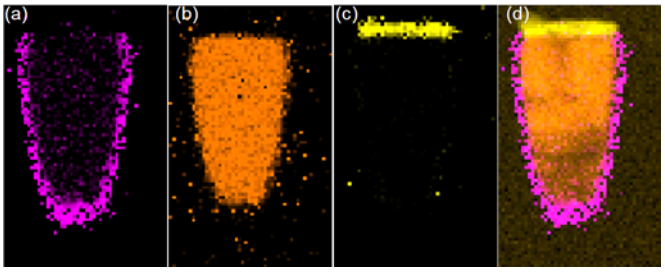

FIG. 6: EDX mapping showing detected (a) Ta at sidewall of the Cu line, (b) Cu, and (c) Co at top surface of the Cu line. (d) Color overlay showing Co covering the Cu surface.

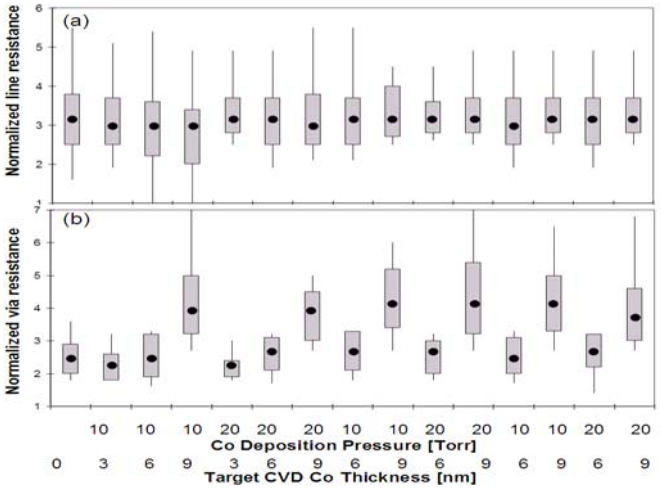

FIG. 7: (a) Line and (b) via resistance measurements .

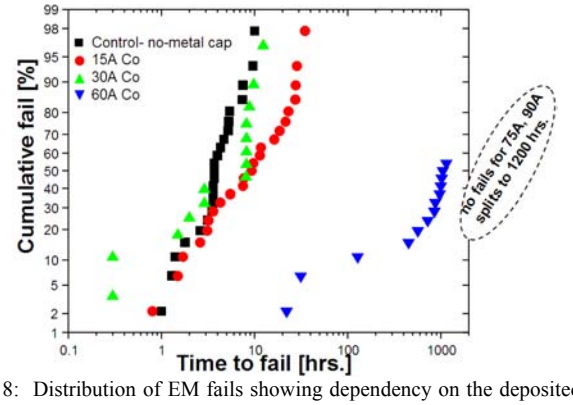

FIG. 8: Distribution of EM fails showing dependency on the deposited Co cap thickness.