NANOCHIP FAB SOLUTIONS
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STRONG ENGINEERING FOUNDATION SUPPORTS YIELD IMPROVEMENT

Yield is the single largest contributor to the financial performance of a semiconductor fab. Yield loss during a new technology or product ramp costs the industry as a whole billions of dollars annually, or tens of millions of dollars per fab. But in addition to the poor yield results themselves, yield losses impair the rate of learning because scrapped wafers or confounded results require additional learning cycles, thus further contributing to loss in time-to-market and in revenues. A fast learning rate is a requirement for high-achieving fabs.

BY HELEN ARMER

APPLIED MATERIALS®

According to Patrick Fernandez, director of Applied Materials' FabVantage Yield Consulting Practice, a large majority of yield loss is due to process and equipment behavior. The remainder is due to device design issues, process integration marginality, manufacturing errors, and facilities problems such as airborne molecular contamination.

Process tools are deterministic: for a given set of process and equipment inputs, the on-wafer result can be derived from engineering or statistical models that are verified with physical understanding. Thus, the majority of yield problems can be solved by fixing issues on the process tools. For example, a fundamental driver of a high density plasma (HDP) process is the deposition-to-sputter ratio. If deposition and sputtering are not optimized, the deposited film can pinch off the entrance to the "gap" (a recessed region that, in cross-section, looks like a via). The result is an incompletely filled gap. This defect, known as voiding, causes electric current leakage, a yield killer. Figure 1 illustrates such a void.

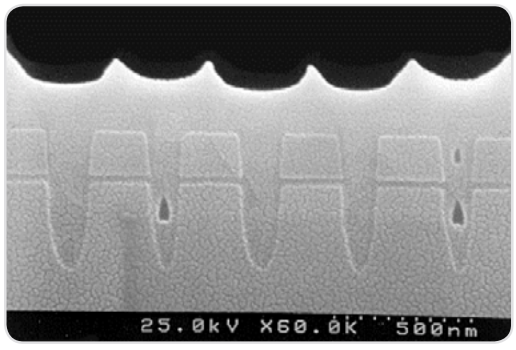

Figure 1. Illustration of a void caused by deposited film pinching off the entrance to the gap in an HDP gapfill process.

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Process and hardware characterization of an Applied Materials HDP chamber identified process regimes that give a void-free gapfill as a function of the structure's aspect ratio (see figure 2a). This model, combined with other process characterization on this chamber, can be used to troubleshoot a void problem. Figure 2b illustrates a second characterization model needed to optimize this process on a given set of hardware.

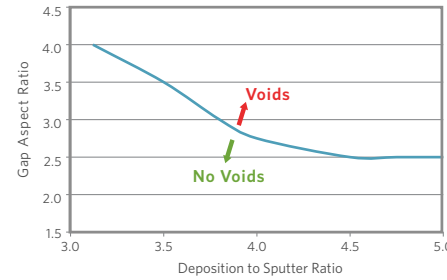
In all, seven process parameters need to be simultaneously optimized to produce a high-yielding structure. While this example is simplistic, it illustrates the extent of process characterization needed to identify and correct misprocessing on a tool and thereby eliminate yield problems caused by process and equipment.

KNOWLEDGE BUILDS BETTER YIELD FROM BOTTOM UP

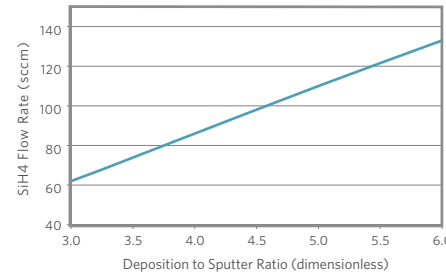
Conventional yield improvement methodology is essentially top-down: start with the outputs—low-yield and non-yielding wafers—and attempt to determine which process steps are the root cause. One problem with this approach is that failure is observed at the end of the line (after hundreds of process steps) or much farther down the line, and weeks may have elapsed since the wafer was misprocessed. During this time, the tool could have been changed, such as by doing preventive maintenance (PM), and the problem may have been fixed.

Usually, it is difficult to identify the root cause. Fabs still have the historical statistical process control (SPC) or fault detection (FD) data for the tool, and this is used to perform root cause analysis, but the root cause may remain elusive if the SPC models are not tracking the correct sensors or if the control limits are not correctly set for detecting yield-detracting excursions. Furthermore, traditional SPC and FD models present their own problems related to the large amounts of data collected and acted upon, alarms, and false positives or negatives (see the article "Software Is Key To Effective Yield Management" elsewhere in this issue).

In addition to these top-down methods, the Applied Materials FabVantage consulting group offers this bottom-up approach: ensure that the process and equipment inputs are optimized for the intended result. The bottom-up approach requires a methodology for identifying the suspect processes and equipment, no small task in a fab that contains hundreds of tools running hundreds of process steps. FabVantage uses a rigorous methodology that was developed



(2a) Process regime that gives void-free gapfill on HDP chamber.



(2b) Model to tune the process to achieve a target deposition-to-sputter ratio.

Figure 2. Process characterization models for the HDP process.

over many years of experience and builds on our vast tool and process knowledge. Some examples of our methodology are:

- **Benchmark each tool against best-in-class data from our knowledge base.** Benchmarking is used to identify tools with poor defect performance and high unscheduled downtime, both of which flag potential yield loss.
- **Review parametric failure paretos.** These may show manifestations of failures that have previously been documented. For example, high transistor leakage variation is sometimes associated with poor temperature control on rapid thermal processing (RTP) spike anneal tools.
- **Study customer inputs and the history of what they have tried.** Customers can often isolate problems to a few tools or modules based on factors such as chamber mismatch, high downtime, and difficulty recovering tools after maintenance.
- **Review failure paretos and wafer-level metrology data from tools with the most failures.** For example, if a CVD tool is being taken down frequently for faceplate or liquid flow meter issues and we see marginal thickness or thickness uniformity performance, then we have a suspect tool. This tool may be running an unoptimized recipe or it may have incorrect equipment constant settings or hardware setup, or perhaps it is not being properly maintained.

As the above discussion of methodology suggests, the knowledge base is one of the critical capabilities of the FabVantage approach. The Applied knowledge base is our extensive compilation of tool performance metrics and best known methods (BKMs). It contains data on each tool's entitlement for uptime, throughput, process results on the wafer, and particles. It contains BKM recipes, equipment constant settings, maintenance procedures, hardware configurations, and software revisions for >500 kinds of process chambers.

Additionally, the knowledge base contains process trend charts that show process sensitivity to the various controllable inputs and that show regions of process marginality. According to Fernandez, "It is difficult to troubleshoot yield problems without understanding these fundamental drivers. We have seen incorrect recipe or equipment setup that has resulted in many wafers being scrapped."

A common example of faulty equipment setup is incorrectly set mass flow controller verification and correction factors. These can result in flow errors of up to 10% and cause a process to operate on a cliff. Other problems frequently encountered include overcleaning during in-situ cleans, resulting in particle generation; underseasoning, causing a wafer-order effect; and running a process with the throttle valve fully open, preventing pressure control.

Older fabs have the challenge that they are typically operating with legacy tools and processes. They may not have the latest process BKMs or maintenance BKMs and their tools may no longer be set up correctly for the processes that are currently run. Leading-edge fabs face a different challenge. While they typically have new or nearly new equipment, overseen by very capable engineering teams, they often need to operate the tool at the edges of the process window in order to push the device performance envelope. Understanding the process chamber's behavior helps show at what point yield is likely to break down, or where the trade-off between device performance and process stability lies.

YIELD IMPROVEMENT IN ACTION

The bottom-up methodology discussed above was used in a recent FabVantage customer engagement. A customer was having yield issues resulting in a large gap to world-class yield performance. The yield loss was believed to be associated with new technology introduction, but the root causes were not readily apparent to the customer. FabVantage benchmarking and assessment identified issues related to transistor control and defects. Further, the yield loss was traced to a small set of tools, including RTP. Subsequent detailed assessments of these tools identified faulty equipment, incorrect equipment setup, recipes missing critical steps, and overcleaning during in-situ cleans.

A joint task force between Applied and the customer was formed. The team set inline targets with weekly reviews. A golden tool approach used split lots to verify and qualify improvements. Inline improvements were achieved within three months, and over the following year yield improved significantly.

While a full discussion of the issues found is beyond the scope of this article, the RTP analysis is typical. As a first step toward better RTP performance, the team discovered that the tools' characteristic fingerprints were far from expected baselines, and that process BKMs were not being used. For example, the temperature sensor trace comparison revealed a large temperature variation (far exceeding recommended range) between zones during the temperature ramp up step, as illustrated in figure 3a. This was determined to be the root cause of the substantial within-wafer variation in transistor characteristics reported by the customer.

Resolution of this issue included improvements in maintenance procedures and a recipe change, resulting in a much tighter temperature range during ramp (see figure 3b) and tighter transistor performance. When the root causes were corrected, the temperature spread dropped to the specification of <50°C (see figure 3b).

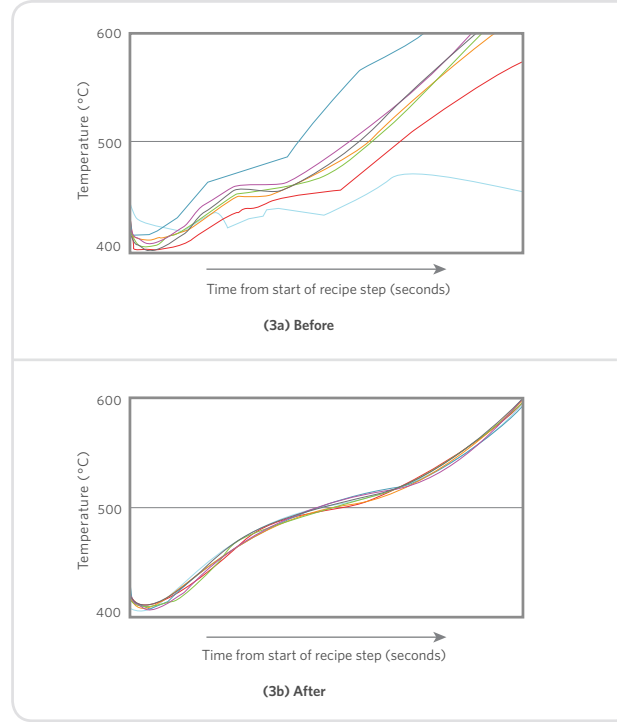


Figure 3. Each color in above figures represents one of seven heater zones in the RTP tool. (3a) shows large within-wafer non-uniformity during the RTP ramp. Once BKMs were implemented, the temperature spread dropped significantly to <50°C (3b).

CONCLUSIONS

Yield is the most serious problem affecting fab productivity, and often it is one of the most challenging to solve. However, with the right approach and information, it is also an eminently solvable problem. Fundamentally, yield loss occurs when a tool fails to apply the correct process to a wafer. Though the number of inputs to any given process is large, most semiconductor manufacturing equipment is well characterized. Systematized knowledge, rigorous audit and analysis methodologies, and deep tool expertise can bring dramatic yield improvement results.

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