

Device performance and yield - A new focus for ion implantation

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Abstract

Recent innovations in ion implantation technology that overcome scaling barriers at 32nm/22nm are reviewed. Some of the hardware improvements will be discussed, but the main focus will be on the process and device data that demonstrates their advantages. These innovations include a cryogenic implant capability that enables a significant reduction in implantation induced crystal damage, molecular implants that show device performance improvements and that use standard ion sources, and various approaches that improve implant performance, particularly when diffusion-less anneal is used.

1. Device scaling trends

Although implant became more challenging with each transition in prior nodes, the change has been fairly monotonic. Energies have gradually reduced, dopant concentrations have gradually increased, both the number and the size of defects have reduced and the number of implants has increased. Until now, the goal of each new generation of implanter has been to meet these gradually evolving requirements with an increasingly productive solution. However, at around the 32nm or 22nm node, a dramatic change is occurring in implant requirements.

Scaling for faster and smaller devices has gradually driven allowable resistance and junction size down to the point where it is no longer possible to achieve the required doping concentrations with the

required levels of dopant activation and diffusion without some major changes in process techniques.

A. Diffusion and Activation

Changes are required to both the implant and anneal processes to reduce diffusion during the post-implant activation/recrystallization process. Changes are also required to both processes to increase dopant activation and decrease resistance.

B. Residual Damage

Since the anneal thermal budget needs to be reduced to minimize diffusion, the implant process needs to be improved to result in less crystal damage, otherwise interface quality and leakage will suffer.

C. Contact Resistance

Scaling has driven contact areas down to the point where contact resistance (R_c) and the limitations imposed by Schottky barrier height constitute a large fraction of the device series resistance. Therefore, process changes are required to reduce contact resistance.

D. Energy contamination and angle control

Since the process requires less diffusion, little smearing of dopant distributions will occur, and so the deleterious effects of energy contamination are more pronounced. Implant therefore needs to find solutions other than deceleration to address productivity at low

energies. Tighter control of implant angle variations is also required for the same reason.

2. Implant innovations to satisfy scaling trends

These scaling trends have driven significant change to implant and anneal technology. Increased activation and reduced diffusion during anneal have resulted from increased peak temperatures but reduced thermal budget. Higher activation is achieved with high temperature pulses that take the silicon surface near to melting temperatures. Lower diffusion results from these pulses being a millisecond or less in duration. These high temperature anneals are often combined with longer duration, lower temperature anneals that attempt to improve recrystallization, repair damage, and provide some lateral diffusion for overlap under the spacer. Both laser and lamp based systems have been developed for this [1, 2].

This trend for reduced diffusion and reduced thermal budget has made it even more necessary for implant technology to evolve. Not only does it need to meet scaling requirements, but it also needs to adapt to accommodate lower thermal budget anneals, and therefore increased sensitivity to crystal damage done by implant and to the various anomalies that result in implanted dopant not ending up quite where expected. This paper will focus on these issues and the changes that are happening to implant to rectify them.

A. Molecular Implants

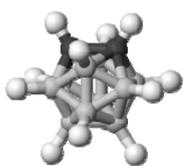


FIGURE 1. Molecular structure of Carborane.

Instead of doping with boron, molecular ions have been developed for certain low energy applications. BF_2 has of course been around for a while. In the last few years larger molecules have been introduced, such as decaborane, octadecaborane, and carborane ($\text{B}_{10}\text{H}_{14}$, $\text{B}_{18}\text{H}_{22}$ and $\text{C}_2\text{B}_{10}\text{H}_{12}$ respectively). Of these,

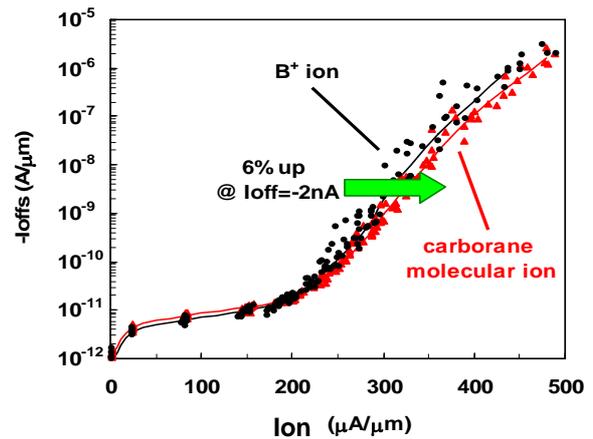


FIGURE 2. Ion/ I_{off} is improved by 6% in a 45nm logic device when carborane is used instead of B^+

carborane is particularly noteworthy because its stable structure (figure 1) allows it to run on a standard ion implanter [3].

For n-type dopants molecular forms of arsenic and phosphorus (As_2^+ , As_3^+ , etc.) have also been examined [4]. The usefulness of these is less obvious because most benefit would be expected when replacing lower mass (sub-amorphizing) implants with molecules.

Molecular ions may be used to increase productivity and to improve device performance. This increased productivity is because at low energies beam currents are usually limited by space charge effects [5]. When beam transport is the limiter, molecular ions may have higher currents because, for the same effective implant energy, molecular ions are implanted at higher energies. Also a single charge is carried over more than 1 dopant ion further reducing space charge.

The improved device performance may come as a consequence of a number of factors. In the case of carborane a large molecule with 10 boron atoms is implanted which, for the same dose, causes more rapid amorphization and lowers residual damage. Also, 20% carbon is simultaneously co-implanted which further hastens amorphization and also improve diffusion and surface activation (see 2.C). Even for 45nm technology, carborane has demonstrated an advantage over boron for logic devices (figure 2) [6]. Sub-32nm devices further

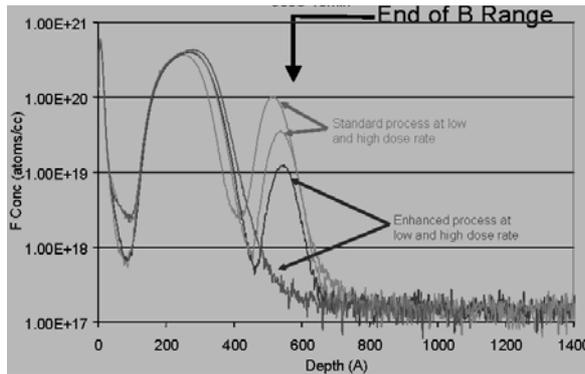


FIGURE 3. Fluorine SIMS of a BF_2 (30keV, 2×10^{15}) implant after a 15 minute, 900°C anneal.

validated strong device improvement using CBH molecule [7].

B. Cryogenic Implants

The importance of substrate temperature during implant has been known for some time [8]. At low temperatures the lattice energy is reduced along with its ability to recover, thereby accelerating the rate of lattice disruption caused by implant. Under these conditions implant amorphizes more rapidly and interstitials tend to remain trapped within that amorphous layer. During anneal, the amorphous layer will readily re-crystallize and fewer residual defects will be left at the end of range (beyond the amorphous/crystal interface). From materials science point of view this effect is well known. As the implant gets colder there will be less dynamic annealing and fewer interstitial defects [8, 9]. This effect is illustrated in figure 3, which shows the fluorine

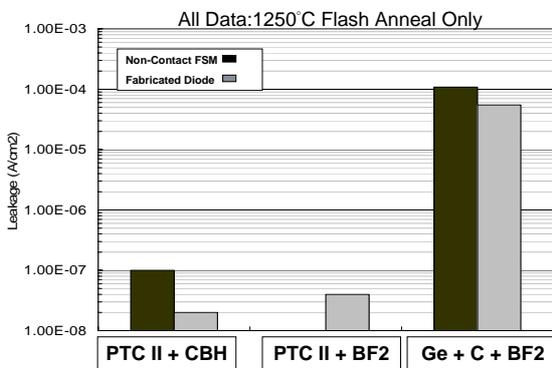


FIGURE 4. Leakage currents from non-contact FSM measurements and from fabricated diode structures.

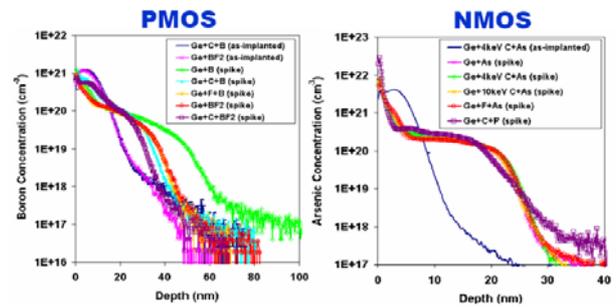


FIGURE 5. Effect of fluorine and carbon co-implants on pMOS and nMOS dopant diffusion.

concentration after a low temperature soak anneal of a BF_2 implant. Fluorine diffuses during the anneal collects at the damage sites. In the case of a room temperature implant it can be seen that a large dose of fluorine decorates the end of range. As the temperature is reduced, this decoration is also reduced until at -100°C , end of range damage is undetectable.

The impact that the removal of residual defects has on leakage current was evaluated by looking at non-contact FSM data as well as diode test structure leakage currents (in conjunction with the University of Surrey) for implants done at room temperature and at -100°C [10]. The results (figure 4) show a dramatic reduction in leakage current at the lower temperature (PTC II is VSEA's trade name for cryogenic implant).

C. Co-implantation

Co-implanting impurities along with the desired dopant has become a popular technique for dealing with the problems of anomalous dopant diffusion and activation during anneal [11].

For example, in pMOS, carbon and fluorine co-implants have been used to both reduce diffusion and increase activation of boron. This is illustrated in figure 5 [12]. Boron diffusion (with a spike anneal) is reduced with both F and C co-implants. This is because the back-streaming interstitials are trapped by the F or C to prevent transient enhanced diffusion of the boron and can inhibit the formation of boron-interstitial clusters that reduce the activation realized.

Carbon co-implants have also been used for nMOS. A carbon co-implant will reduce diffusion of phosphorus, for example, as is shown in figure 5.

Co-implantation has not only benefited the performance of pMOS source drain extension, but also the nMOS contact region (as will be discussed next). This technique is also being used to produce super steep p-type halos. The use of C or N co-implantation for this has been discussed recently [13, 14].

D. n-Type contact implants

n-Type contacts have been made using As⁺ implants. However, as scaling has reduced contact areas, higher active dopant concentrations are required to reduce series resistance. Phosphorus is a good candidate for this as it has higher solubility than arsenic. However, phosphorus suffers from high diffusivity. Carbon is known to reduce this, however silicon has traditionally needed to be fully amorphized for the C to have full effect [11]. Unfortunately, traditional PAI would cause high EOR damage and excessive leakage. However, recent developments demonstrate that if the C co-implant is performed at -100°C, then no pre-amorphization is needed and very abrupt and low resistance contact junctions can be achieved (figure 6).

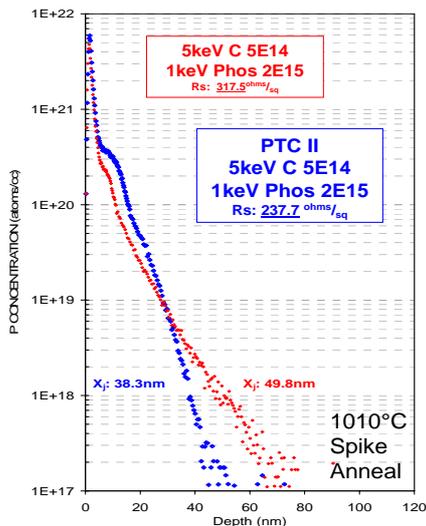


FIGURE 6. SIMS showing that the diffusion of phosphorus is better controlled by a carbon co-implant when the implants are done at -100°C.

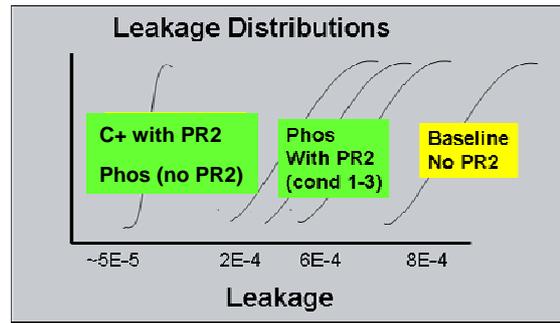


FIGURE 7. 32nm LP logic data showing devices made with -100°C C⁺ & P⁺ contacts had much lower junction leakage than those using the As⁺ POR.

An additional problem with arsenic contacts has been EOR damage induced leakage. Figure 7 shows a declassified representation of data on 32nm low power logic devices where leakage was reduced by more than an order of magnitude because residual damage was reduced when the arsenic baseline was replaced with a cold C and P implant.

E. Pre-silicidation implants

Nickel silicide is used to reduce contact resistance to the source and drain. However, this faces many challenges such as controlling Ni diffusion, optimizing the silicide/silicon interface, avoiding Ni pipping (usually along implant induced damage sites) and controlling agglomeration, particularly in the SiGe strained layer making pMOS especially challenging [15].

A pre-silicide implant is one way of addressing some of these problems. For nMOS, diffusion of Ni during the silicidation step is reduced by using a Si implant to pre-amorphize the contact area. For pMOS, carbon has the same effect and the added advantage that it also limits Ni diffusivity by getting interstitials. However, the depth and abruptness requirements of that C implant have made it impossible to amorphize until cryo implantation was developed. Figure 8 shows how nickel silicide is formed at lower temperatures, with better thermal stability and with lower sheet resistance when it is preceded by a -100°C carbon implant.

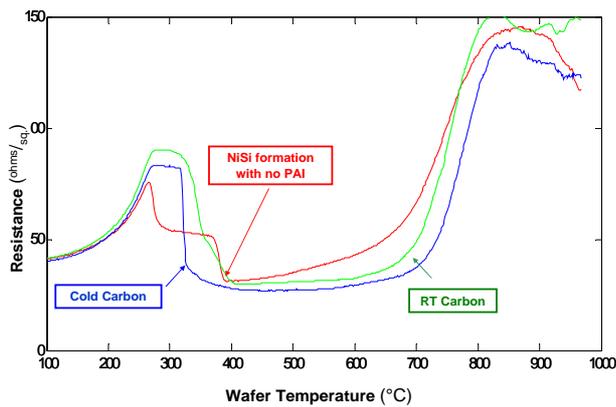


FIGURE 8. Structured wafers results for silicide resistance when preceded by a) no implant (red), b) a room temperature 1keV C 1e15 implant (green), and c) the same C implant at -100°C (blue)

The cold carbon pre-amorphizing implant also shows a significant benefit to the agglomeration and interface smoothness problems. Figure 9 shows atom probe results for nickel silicide formation with (bottom) and without (top) the -100°C pre-amorphizing implants. It can be seen that the cold implant prevents the agglomeration of Ge in this strained contact. Moreover, the silicide/silicon interface is considerably smoother.

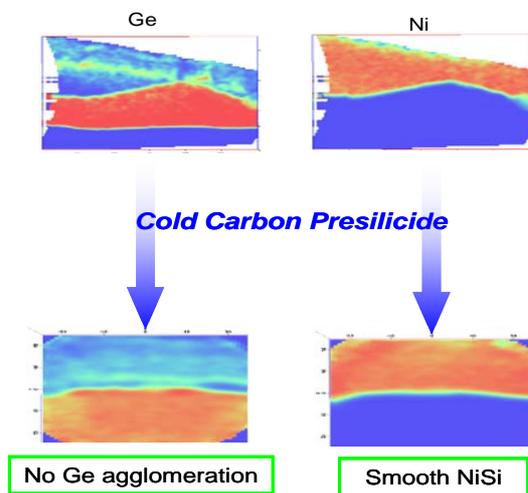


FIGURE 9. Atom probe results showing Ge (left) and Ni (right) distributions highlighted in red/orange. Data is taken after silicidation with (bottom) and without (top) a -100°C carbon pre-amorphizing implant

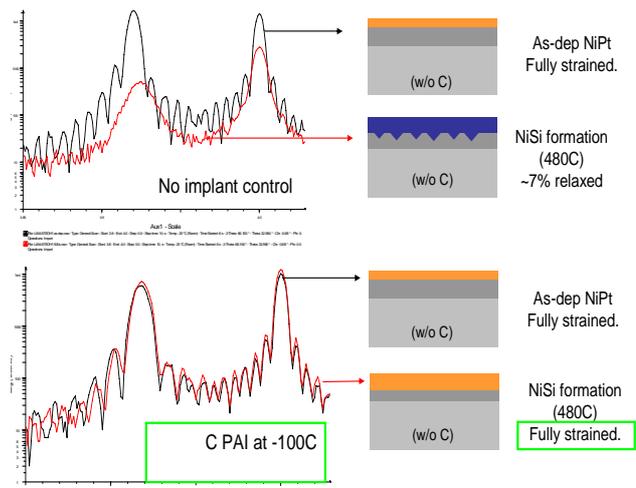


FIGURE 10. XRD Comparison of as-deposited strain (black) to post silicidation strain (red) with (bottom and without (top) a -100°C carbon implant

Presumably as a consequence of preventing germanium agglomeration, the as-deposited strain is fully retained after the silicidation step when the process is preceded by a -100°C carbon implant, but is lost when not. This is shown in figure 10.

So, a cold carbon pre-amorphizing implant alleviates many of the issues suffered by silicidation. This implant allows a more stable silicide to form, with lower resistance and without strain loss for pMOS. The final impact on device yield and performance will be discussed at this conference [16].

F. Tighter Angle Control

The implanted beam angle can vary for a variety of reasons, but generally manifests itself in one of three ways. Firstly there may be a ‘global steering angle’ that results in a wafer-to-wafer variation in implant angle. The most common cause of this might be beam tuning repeatability. Secondly may be a ‘local steering angle’ which results in within-wafer angular variation. This may be caused by beam angle variations across a ribbon beam or by incomplete exposure of a wafer to a spot beam. Finally, there will always be some amount of ‘within-device angular spread’. This occurs because, even if the beam set up is completely repeatable and

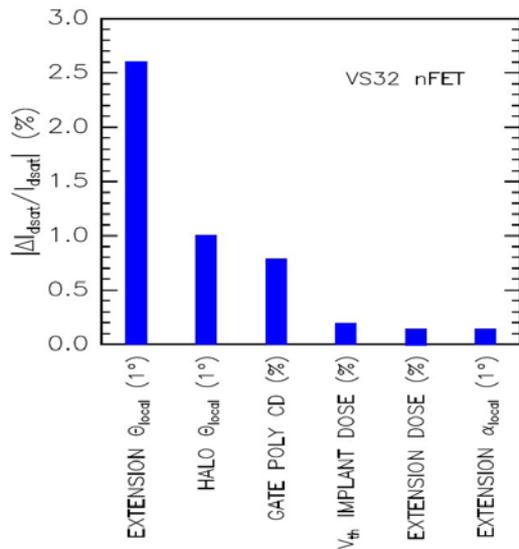


FIGURE 11. TCAD results for a 32nm nFET device showing drive current variability as a function of various implant errors.

invariant, all points on the wafer will be implanted with some spread of implant angles.

Implanters have always suffered from these angle variations, however they have not had significant impact because device geometries have not been that sensitive and because diffusion during anneal has smeared out much of this variation. Starting with ~32nm half-pitch devices this is no longer the case and small changes in implanted profile are beginning to have a significant impact on device characteristics.

For a 32nm half-pitch nFET, as little as 1° of beam steering angle during the extension implant leads to a 3% reduction in I_{dsat} [17]. In fact, extension beam steering is the largest contributor to I_{dsat} degradation, ahead of halo implant beam steering, gate-poly CD variations, or implant dose (figure 11). It is therefore imperative that beam steering and beam parallelism are well controlled to achieve high yield in the production of advanced HP technology.

Some very sophisticated angle measurement metrology and beam angle tuning technology has been developed over the last few years that meet this challenge by providing a 0.1° angle repeatability performance [18]. Quad implants also significantly

reduce the impact of beam steering on device performance. However this can have a significant impact on throughput unless the wafer is held on a platen that can be rotated.

3. Conclusions and Summary

We have presented the device performance and yield challenges to ion implantation resulting from advanced semiconductor scaling and the technology developed to address them. Cryogenic implants, molecular species and precise angle control have been employed to produce reduced damage ultra-shallow junctions, low leakage devices, and improved nickel silicide required for 32nm/22nm device scaling.

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