Device Scaling and Performance Improvement: Advances in Ion Implantation and Annealing Technologies as Enabling Drivers

Yuri Erokhin

Applied Materials - Varian Semiconductor Equipment, 35 Dory Road, Gloucester, MA 01930, USA
Tel: 1-978-282-2704, Fax: 1-978-281-1897, E-mail: yuri_erokhin@amat.com

Abstract

The complexity of ion implant applications in IC fabrication has grown significantly since becoming the preferred process for doping semiconductors. Aggressive device scaling over the last decade raised unique challenges. This resulted in the invention of novel implant applications to address device scaling driven issues and the development of new generations of ion implanters. These newly developed tools are capable of delivering a wide variety of ion beams of traditional doping and non-doping species, with manufacturing worthy beam currents over an energy range extending from 200 eV to several MeV. They are capable of controlling implanted wafer temperature down to cryogenic conditions to take full advantage of new defect engineering approaches. All these innovations resulted in significant growth of ion implantation steps in advanced IC manufacturing for both doping and **P**recision **M**aterials **M**odification (PMM). In this paper we present an overview of recent advances in ion implantation technologies and applications addressing sub-20nm device and process integration challenges. We illustrate how these innovations enable improvement of device performance and expansion of process margins through novel capabilities of ion implantation tools coupled with innovative materials engineering approaches for junction formation and for process modules beyond of traditional doping applications.

1. Device Scaling Challenges

Scaling of planar bulk silicon devices past 32/28/22nm nodes presents major challenges in three key device performance and yield areas: (i) escalating device leakage, (ii) increased Source/Drain contact resistance and (iii) increased device variability and narrowed margins of device manufacturing processes.

A. Device leakage

Rapidly escalating device leakage is a critical issue having its most severe impact on SOC ICs targeting mobile applications. Root causes for increased leakage in scaled down planar bulk silicon devices are attributed to several scaling factors. First, the inability to scale down V_{dd} proportionally with device channel length (L_g) increased the magnitude of the electric field in the SD-halo device regions leading to rapidly increasing **G**ate **I**nduced **D**rain **L**eakage (GIDL), **B**and-**T**o-**B**and-**T**unneling (BTBT) and **S**hort **C**hannel **E**ffects (SCE). Secondly, a requirement to minimize dopant diffusion in scaled down devices and to meet ever higher requirements for SDE junction abruptness imposes severe limitations on the allowable thermal budget for the post implant anneals. Typically, at the 20nm node peak sRTA temperature have to be set at sub-1000 ^{o}C. This results in the inability to adequately anneal implantation induced crystal damage and further increases device leakage due to charge traps in the junctions depletion regions related to un-annealed crystal defects.

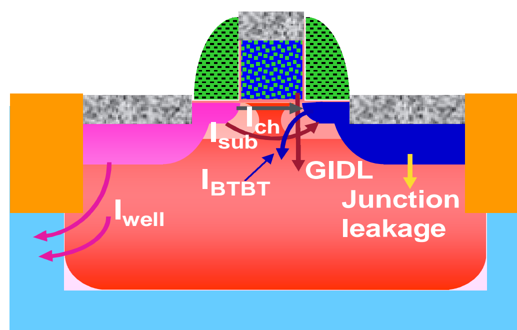
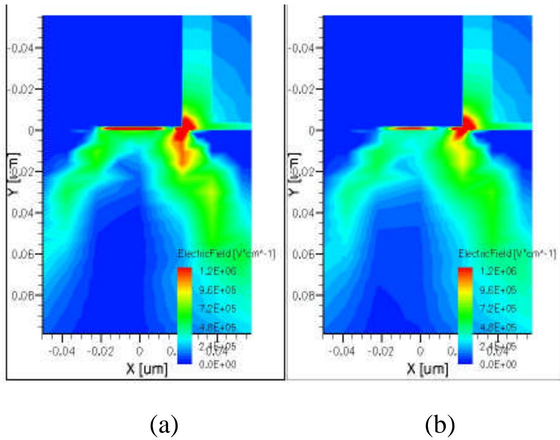


Fig. 1. Key leakage path in planar bulk silicon sub-32/28nm devices.

To at least partially mitigate the above effects a combination of process engineering and novel implant technology capabilities are deployed at sub-32/28 nm nodes. From a process engineering standpoint minimization of leakage is accomplished by careful optimization of dopant distributions in the SD/halo regions to provide optimum suppression of SCE while minimizing the electric field especially in the SDE/Halo device regions. To achieve this, the BF_2 halo implants traditionally used in NMOS devices are being replaced with In and B with carbon co-implant to further suppress boron diffusion.



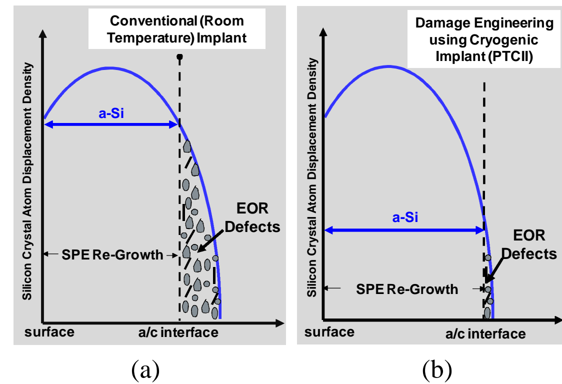
(a) (b)

Fig. 2. TCAD modeling of peak electric field in the drain/halo NMOS device region with (a) optimized one-step BF_2 halo implant vs. (b) halo formed using optimum Indium, Boron and Carbon implant sequence.

As seen in Fig. 2, a multistep halo implant confines the area of maximum electric field in proximity to the gate edge. This reduces the GIDL and BTBT components of the device leakage current compared to a traditional one-step BF_2 NMOS halo implant.

Further leakage reduction is enabled by halo and SDE implants done at cryogenic temperatures. By changing from room temperature to cryogenic silicon wafer temperature a significant reduction of **E**nd-**o**f-**R**ange (EOR) damage in implants near amorphization conditions in silicon has been demonstrated by Suguro *et al* well over a decade ago [1]. The practical relevance of this approach for resolving critical device scaling challenges reached its critical mass when the IC industry approached the 45/40nm node. A production-worthy implant tool capable of implanting wafers at cryogenic temperatures down to -100 ^{o}C had been first introduced by Varian [2]. Theoretically, defect improvement efficiency could have been even higher at wafer temperatures below -100 ^{o}C, but process integration limitations, specifically those related to photoresist properties, set the optimum wafer temperature for cryogenic implants at about -100 ^{o}C.

The materials science phenomenon responsible for EOR reduction enabled by implants at cryogenic temperatures is illustrated in Fig. 3 below. It exploits a well known effect of the temperature dependence of the accumulation of implantation-induced crystal damage in silicon. Under the same implantation conditions (nuclear stopping energy deposition) the accumulation rate of crystal damage in the silicon lattice increases with reduction of the wafer temperature. For amorphizing implant conditions this effectively results in an increased thickness of the amorphous layer created by the incoming ions, in turn consuming a significant fraction of the end-of-range defects present within the interface region between the amorphous layer and the undamaged Si crystal substrate.



(a) (b)

Fig. 3. Schematic illustrating formation of amorphous vs. sub-amorphized (EOR) regions in Si created by amorphizing implants at RT (a) and cryogenic (b) implant conditions.

SDE and halo implants of doping and non-doping co-implant species at cryogenic wafer temperatures enable a reduction of those components of device leakage that are related to residual, implant induced defects. Cryogenic implants also reduce device variability by minimizing dopant transient enhanced diffusion that is largely influenced by EOR damage.

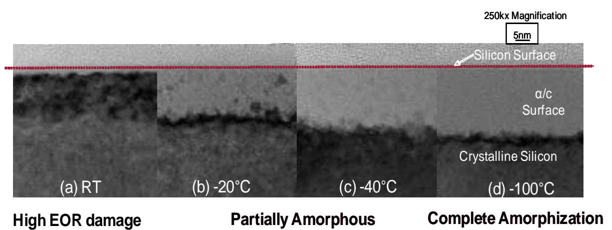
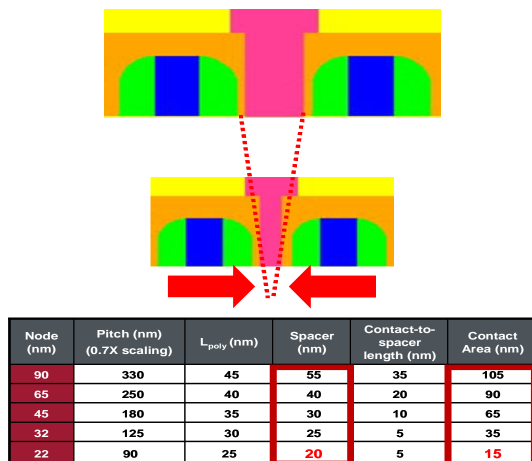


Fig. 4. XTEM of Si wafers implanted with 5keV carbon to a dose of 10^{15} cm^{-2} at RT, -20 ^{o}C, -40 ^{o}C and -100 ^{o}C wafer temperature [3].

B. Contact resistance

Achieving a source/drain contact resistance to device low enough to take full advantage of the high PMOS and NMOS drive currents achieved by mobility enhancement techniques emerged as significant scaling challenge in sub-32nm devices. Its impact is projected to be even stronger as devices scale down further.



Node (nm)	Pitch (nm) (0.7X scaling)	L_{poly} (nm)	Spacer (nm)	Contact-to-spacer length (nm)	Contact Area (nm)
90	330	45	55	35	105
65	250	40	40	20	90
45	180	35	30	10	65
32	125	30	25	5	35
22	90	25	20	5	15

Fig. 5. Estimated dimensions of key MOS device elements for various device nodes.

The reason for contact resistance to emerge as a major scaling challenge is illustrated in Fig.5. This figure presents scaling trends for various MOS device elements from the 90 to the 22 nm nodes. Due to MOS device gate length (L_g) and spacer width scaling slower than the 0.7X node-to-node pitch scaling factor the area available for contact via had to be reduced more aggressively than the 0.7X pitch scaling resulting in disproportionate growth of contact resistance. To mitigate this effect significant efforts have been made to reduce sheet resistivity values of the NiSi SD contact area with ion implantation playing a crucial role in already adopted and emerging contact formation processes.

Multiple solutions are being implemented into leading edge sub-32/28nm process integration sequences. One of the approaches relies on a pre-amorphization implant (PAI) of a thin layer of silicon that is designated to be consumed by the subsequent reaction with the deposited Ni to form the NiSi film. This approach is based on the phenomenon where the reaction of Ni with amorphous silicon resulting in formation of the targeted phase of nickel silicide occurs at temperatures lower than that required for crystalline silicon [4]. Such an approach enables improvement of the planarity (morphology) of the interface between nickel silicide and silicon thereby improving silicide sheet resistance and widening the temperature window prior to silicide converting to the higher resistivity $NiSi_2$ phase [5]. PAI when combined with carbon co-implant at -100 °C further improves the interface morphology since the reduced EOR damage and the additional trapping of remaining silicon interstitials by carbon further suppressing NiSi agglomeration and formation of NiSi silicide piping defects [6].

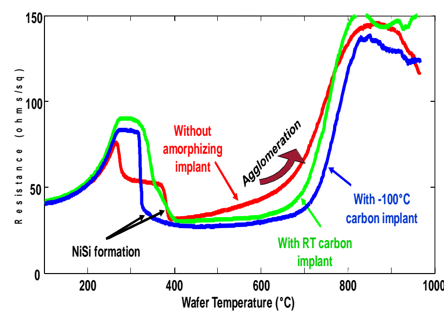


Fig. 6. Structured wafers results for silicide resistance using no implant (red line), and with a 1keV 1e15 cm^{-2} carbon implant at room temp (green line) or -100°C (blue line) [6].

It has been demonstrated that further improvement of the NiSi interface planarity and suppression of piping defects can be achieved by replacing the second soak RTA anneal with a laser anneal in a thermal cycle used to form nickel monosilicide [7].

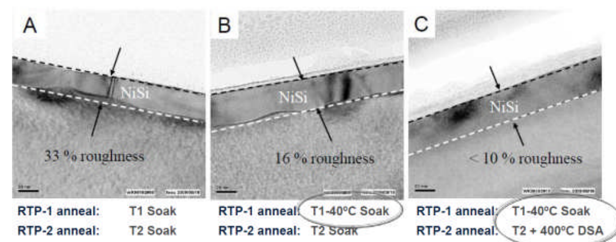


Fig. 7. Improvement of NiSi interface planarity enabled by replacing second soak RTA anneal with Dynamic Laser Anneal (DSA) at elevated wafer temperature and millisecond pulse duration.

Significant opportunity to further reduce contact resistance resides in minimizing the potential barrier (Schottky Barrier Height – SBH) existing between NiSi and the device source/drain regions. To some degree this is achieved by maximizing the concentration of electrically active dopant at the silicide/silicon interface. Yet, the realization of the ultimate improvement opportunity requires metallurgical engineering of the silicide-to-Si interface either by deploying new silicide materials or by incorporation of exotic species at the NiSi/Si interface. Yeo *et al* investigated silicide film resistivities and SBH values for various silicides types. For NiSi SBH is reduced by incorporating a high concentration of dopant at the interface between NiSi and silicon and/or by incorporating into the interface region exotic species such as Al, Se, S [8,9].

Data in Figures 8 and 9 indicate that there is an opportunity for significant SBH reduction in NMOS by implantation of aluminum into the NiSi/nSi

interface region. For PMOS SBH could be suppressed by modifying the properties of the NiSi/pSi interface through combination of PAI, carbon co-implants and Al implant.

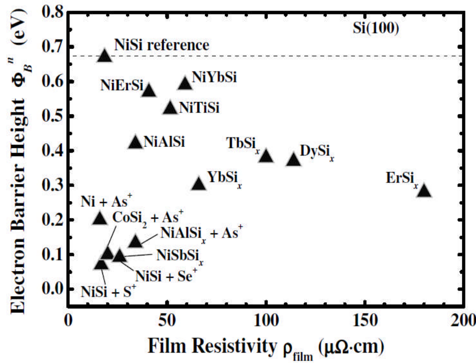


Fig. 8. Electron barrier height $\Phi_B{}^n$ versus film resistivity for various contact silicides formed on silicon. The labels "As$^+$", "S$^+$" and "Se$^+$" refer to samples in which arsenic, sulphur and selenium were implanted prior to silicidation [9].

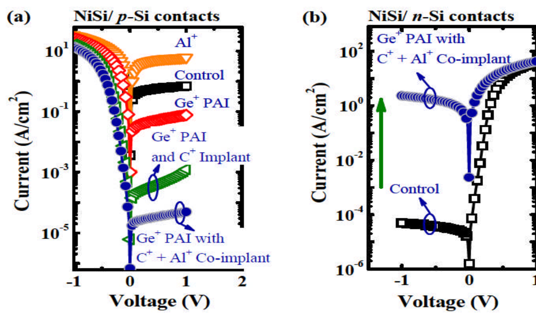
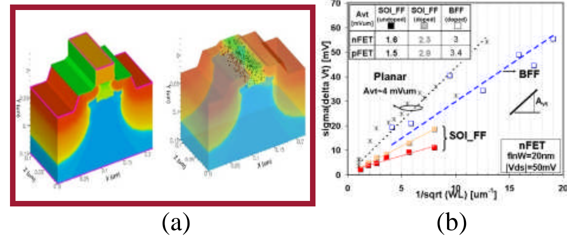


Fig. 9. Impact of various implants on the effective Schottky barrier height. In the absence of Ge PAI and Carbon implant, Al implant reduces the effective hole SBH. In the presence of Ge PAI and C implant, Al implant reduces the effective electron SBH [10].

Overall, as device pitch continues its 0.7X node-to-node scaling beyond sub-20nm nodes, the impact of contact resistance scaling is expected to become only more severe regardless of whether the industry stays with a planar device architecture or is transitioning to FinFET devices. To address the contact resistance issue implanters capable of implanting novel exotic species and performing implants at cryogenic conditions are required.

C. Device and Process Variability

Device variability and narrowing process margins have been identified as another critical scaling issue at the introduction of the 45nm node [11]. As devices scale down the device variability inherently increases both because of fundamental attributes of planar bulk silicon devices and due to the increasing variability of key manufacturing processes.



(a) (b)

Fig. 10. Illustration of stochastic nature of dopant atom placement in device channel (a). V_{th} variation (RDF effects) vs. device channel volume (b) [12].

One source of planar bulk silicon variability is attributed to **R**andom **D**opant **F**luctuation (RDF) effects [12]. RDF effects arise from the fact that as planar devices scale down the number of dopant atoms in the device channel region progressively decreases to the point where sub-32nm devices have only hundreds of dopant atoms in the channel. Even though on a macro scale channel, halo and SDE implants have typically better than 1% 1σ dose uniformity, statistical variations of dopant atoms in channel regions of sub-32nm devices, as illustrated in Figure 10a, could be several times higher leading to inherent progressively increased V_{th} variability as devices are scaled down, see Fig. 10b [13].

In addition to RDF effects that are stochastic in their nature and can only be mitigated through device architectural solutions there are also significant systematic sources of device variability attributable to various device manufacturing processes including ion implantation. Fig. 11 presents a pareto analysis of TCAD-modeled I_{on} sensitivities in 32 nm NMOS devices to a various implant parameters including ion beam angle setting accuracy [6].

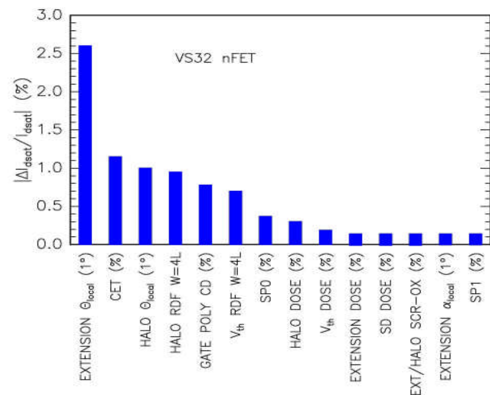


Fig. 12. Pareto analysis of 32nm NMOS device sensitivity to a variety of process variables.

Energy purity (zero or near zero energy contamination) has been realized as an important emerging requirement for both improving device I_{on}/I_{off} characteristics as well as reducing process variability especially for ultra-low energy implants when the beam is typically extracted at initial energies higher than that set in the final implant recipe. Another recently emerged contributor to device variations has been linked to run-to-run changes of beam current density. Beam current density effects on process margins have been attributed to the wide adoption in scaled down device process integration flows of various defect engineering approaches and to the reduction of post implant anneal thermal budgets. A. Lee *et al* reported [14] that implantation of pSD and nSD doping species and of carbon co-implants at cryogenic wafer temperature results, as shown in Fig. 13, in reduced device mismatch (V_t) in DRAM sense amplifiers. It also improves DIBL and GIDL.

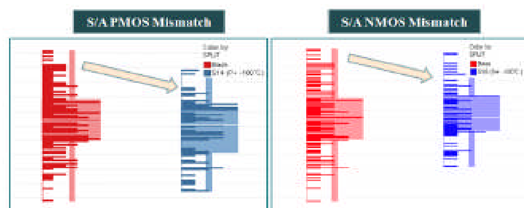


Fig. 13. 11% PMOS and 12% NMOS improvement of V_{th} mismatch in DRAM sense amplifier with pSD and nSD implants performed at cryogenic temperature [14].

D. Implant application for addressing scaling issues and widening process margins in non-doping related process modules.

Materials engineering by ion implantation has been demonstrated to enable widening process margins and reducing the variability in several device fabrication modules not related to transistor formation doping processes. Most notable of those are etch [xxx] and lithography. In the lithography module **L**ine **E**dge and **L**ine **W**idth **R**oughness (LER and LWR) are among the most significant contributors to systematic process variations. One of the recent areas of the development focus is deployment of Precision Materials Modification (PMM) approaches to expand lithography process margin and to reduce LER and LWR [15]. Ion implantation into photoresist masking features has been demonstrated to enable reduction of LER/LWR while having a minimal impact on other important PR feature characteristics – its Critical Dimensions (CD) and Profile [16].

To comprehend the impact of the ion implanted treatment to the resist material, it is valuable to examine the Fourier decomposition of the roughness into the spectral frequency components. The data in Fig.14 shows that ion implantation yields up to 50% improvement in the overall roughness by primarily impacting the mid range roughness but also the low frequency or long range roughness of the patterned image. Depending on the design attributes, significant improvement in mid and low frequency roughness can directly be tied to improvements in device variability.

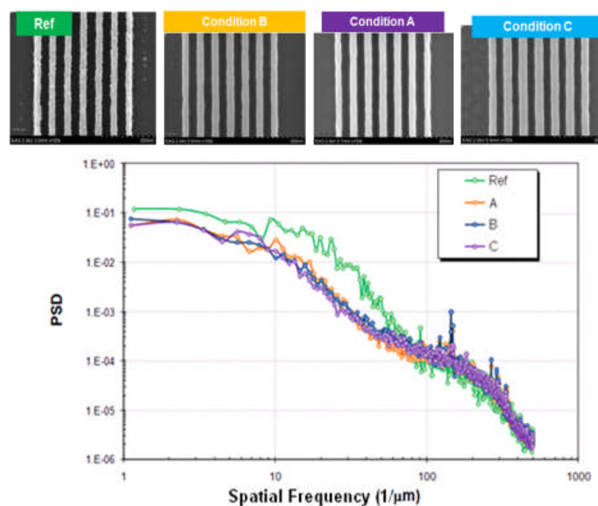


Fig. 14. LER spatial frequency in 193i resist masking features for various implantation treatments. Note LER reduction in mid-range spatial frequencies that are most detrimental for V_{th} variability [16].

E. Advanced Ion Implantation Technology

To take full advantage of the doping and defect engineering approaches described above and of Precision Materials Modification opportunities it is necessary that advanced implant tools for sub-20nm node incorporate a variety of novel features and capabilities. These tools must have ability to perform implants into wafers cooled down to cryogenic temperatures, support implant requirements for a wide array of doping, co-implant and exotic species some with energies down to 200 eV. To expand process margins and reduce device variability leading edge implant tools must have engineered into them beam angle control and correction capabilities to achieve beam angular position accuracy of about 0.1^{o} and have energy filters and capabilities for recipe driven beam current density setting. These leading edge tools must also meet ever tighter particulate and metals contamination control requirements. Figure 15 contains a schematic of the VIISta Trident HC from Applied Materials/Varian Semiconductor Equipment, the latest generation of high current implanters.

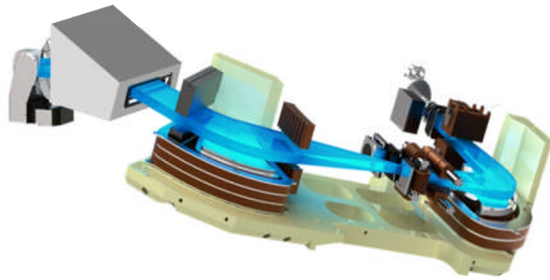


Fig. 15. Example of advanced implanter beam-line architecture (AMAT/VSE VIISta Trident HC). The beam is generated by an ion source and passes through analyzing, angle corrector magnets and energy filter to produce a horizontally uniform ribbon beam for implanting a vertically scanned 300mm wafer that can be cooled down to cryogenic temperatures.

3. Conclusions and Summary

Sub-32nm scaling of planar bulk Si devices presents a set of unique scaling issues. Device leakage, low contact resistance and variability of device characteristics are among the most critical ones. Ion implantation has emerged as one of the most critical IC manufacturing processes enabling sub-32nm scaling. It has an unique ability for precise placement of dopants on the nm scale both for depth and lateral distributions. It provides device designers and process integration engineers with new junction engineering and Precision Materials Modification capabilities. The latest generation of advanced ion implantation equipment incorporates unique capabilities supporting current and emerging requirements for sub-20nm devices.

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