Enabling Effective Work Function Tuning by RFPVD metal oxide on High-k Gate Dielectric

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Abstract

For high-k metal gate integration, one of the major challenges with gate-first flow is to achieve and maintain desired effective work function and EOT after high thermal budget. One way to achieve the desired effective work function is to use dipole effect by adding metal elements into high-k dielectric film [1][2]. Metal oxide cap layer is one of the proven methods for this purpose [3]. The key requirements for metal oxide deposition are to have uniform thin dielectric film deposition with low damage, and minimal EOT change. On the other hand, PVD is known to be a robust process over many technology nodes through thin metal deposition. Also, film material or components can be more easily changed by PVD than by other deposition processes, such as ALD. RF magnetron PVD enables not only dielectric film deposition [4] but also precise thickness control and low plasma damage. Hence, RFPVD is one of the great candidates for cap layer deposition.

In this study, RFPVD process was evaluated for metal oxide cap deposition. Aluminum oxide was selected as the cap layer to adjust effective work function for PMOS devices with hafnium oxide.

MOSCAP devices were fabricated with the process flow shown in Figure 1 on 300mm p-on-p+ wafers with ALD-TiN as the metal gate. AlO_x film was deposited by RF PVD at Endura mainframe on top of HfO_2 film as well as samples without cap layer as reference.

Prior to MOSCAP test, SPIDER [5] wafer test showed no leakage degradation after RFPVD AlO_x process, which confirmed no large charge damage induced by RFPVD.

MOSCAP showed that AlO_x cap layer provided positive V_{FB} shift by about 200mV with good within-wafer uniformity (Figures 2 and 3). The result agrees with a previous report using HfSiO with Al addition [3]. However, the 1.0nm of Al oxide cap layer also caused capacitance equivalent thickness (CET) increase by more than 0.35nm. To minimize CET increase, thinner Al oxide, 0.5nm and 0.3nm, were tested. It was found that 0.5nm AlO_x cap addition achieved comparable V_{FB} shift as 1.0nm with minimal EOT increase, about 0.1nm, as shown in Figure 4. Samples with AlO_x cap layer showed comparable gate leakage current to the reference (Fig. 5). Interface state density, D_{it}, was also extracted by the conductance method. D_{it} with AlO_x was comparable to the reference without cap layer, which confirmed no additional damage by RFPVD process.
Figure 3 also shows the effects of high temperature anneal. V_{FB} shift was comparable without HT anneal. This indicated that HT anneal may not be required to achieve the maximum V_{FB} shift by the AlO_x cap layer.
Thus, RFPVD AlO_x cap layer showed good electrical results in terms of V_{FB} shift, CET, gate leakage, and interface damage.

RFPVD has been confirmed as a good candidate for metal oxide cap deposition to tune effective work function of high-k gate stack. Further study is required to achieve optimal V_{FB} shift with varying metal oxide and thermal budget. RFPVD can be applied for different material depositions by changing the target material, such as La for NMOS devices. Therefore, it is a critical and versatile technique to enable high-k metal gate implementation.

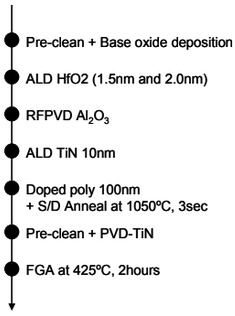

Figure 1 Process Flow

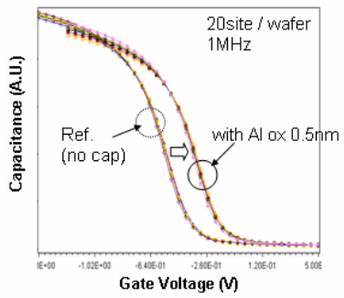

Figure 2 20 site C-V curves with and without RFPVD Al oxide cap layer on 2.0nm HfO_2. C-V curves show uniform V_{FB} shift by AlO_x cap layer across the wafer.

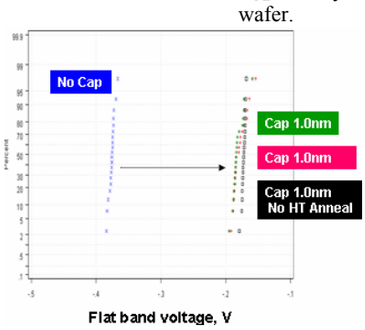

Figure 3 Probability plots of V_{FB} with and without 1.0nm Al oxide cap and HT anneal.

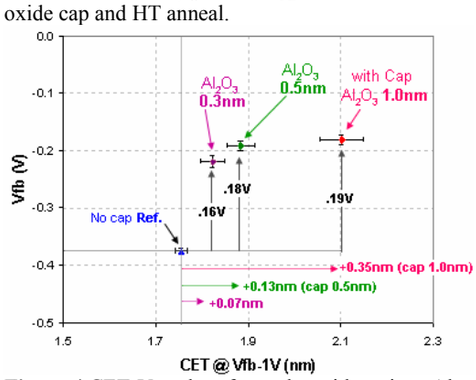

Figure 4 CET-V_{FB} plot of samples with various Al oxide cap thickness; 0, 0.3, 0.5 and 1.0nm on 2.0nm HfO_2. 0.5nm cap shows equivalent V_{FB} shift, ~0.2V, to 1.0nm cap with minimal CET increase, ~0.1nm.

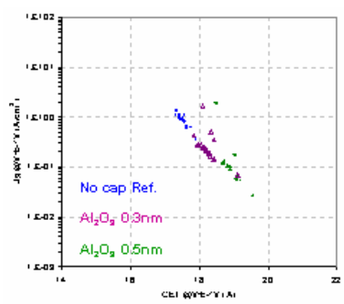

Figure 5 CET-J_g with and without Al oxide cap, with and without AlO_x show comparable gate leakage current.

References

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