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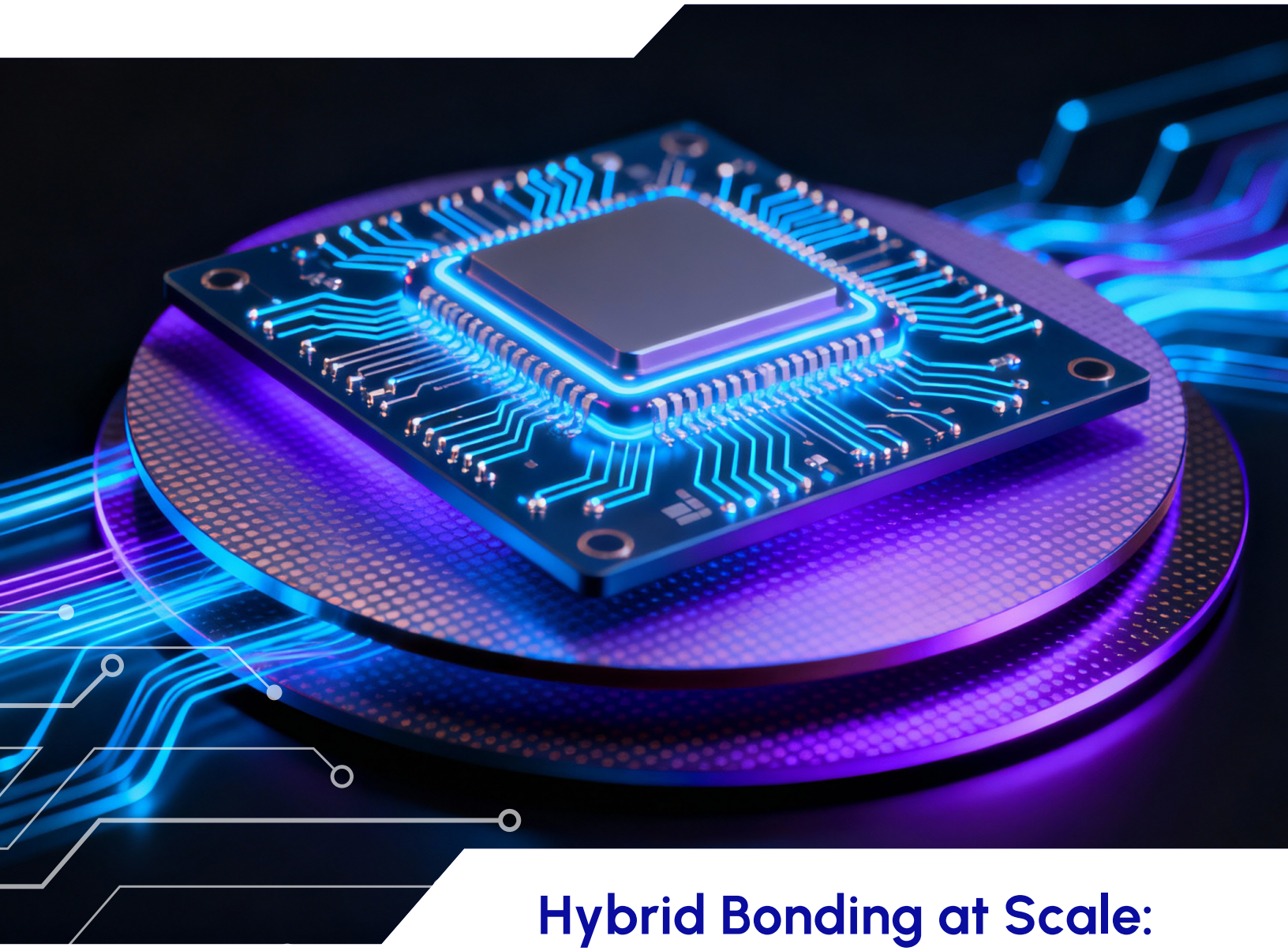


Hybrid Bonding at Scale: Powering the Next Era of Semiconductor Packaging

OCTOBER 2025

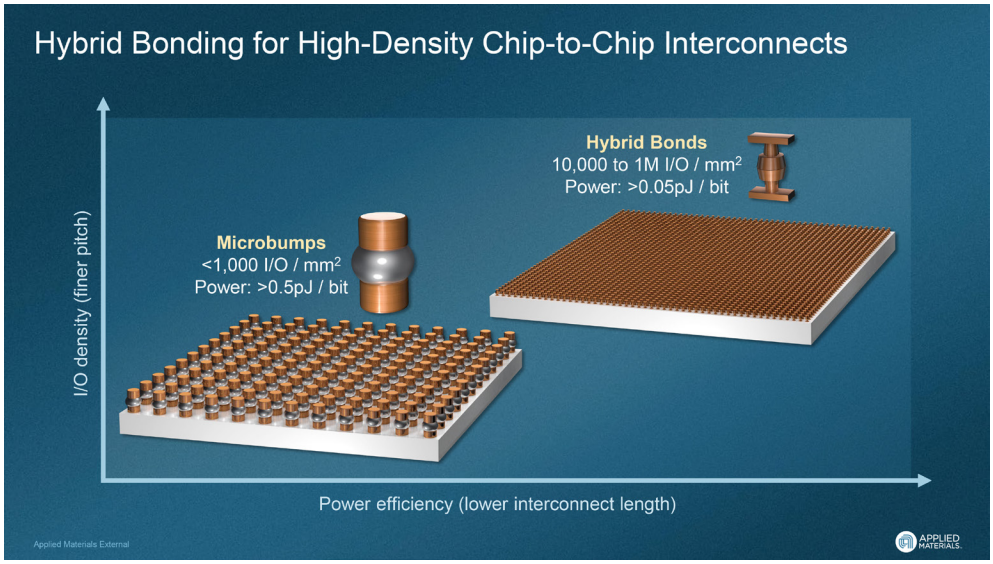
Introduction

Advanced Packaging (AP) has become the cornerstone of semiconductor scaling in the AI era. As transistor-level improvements face physical and cost limitations amid the slowdown of Moore's Law, AP technologies now drive performance, power efficiency, and integration density. This market brief explores the critical role of **Hybrid Bonding (HB)**, Applied Materials' leadership in AP, and its upcoming **Kinex platform (developed in partnership with Besi)** that addresses the bottlenecks in hybrid bonding for the future of semiconductors.

Why Advanced Packaging and Hybrid Bonding Matter

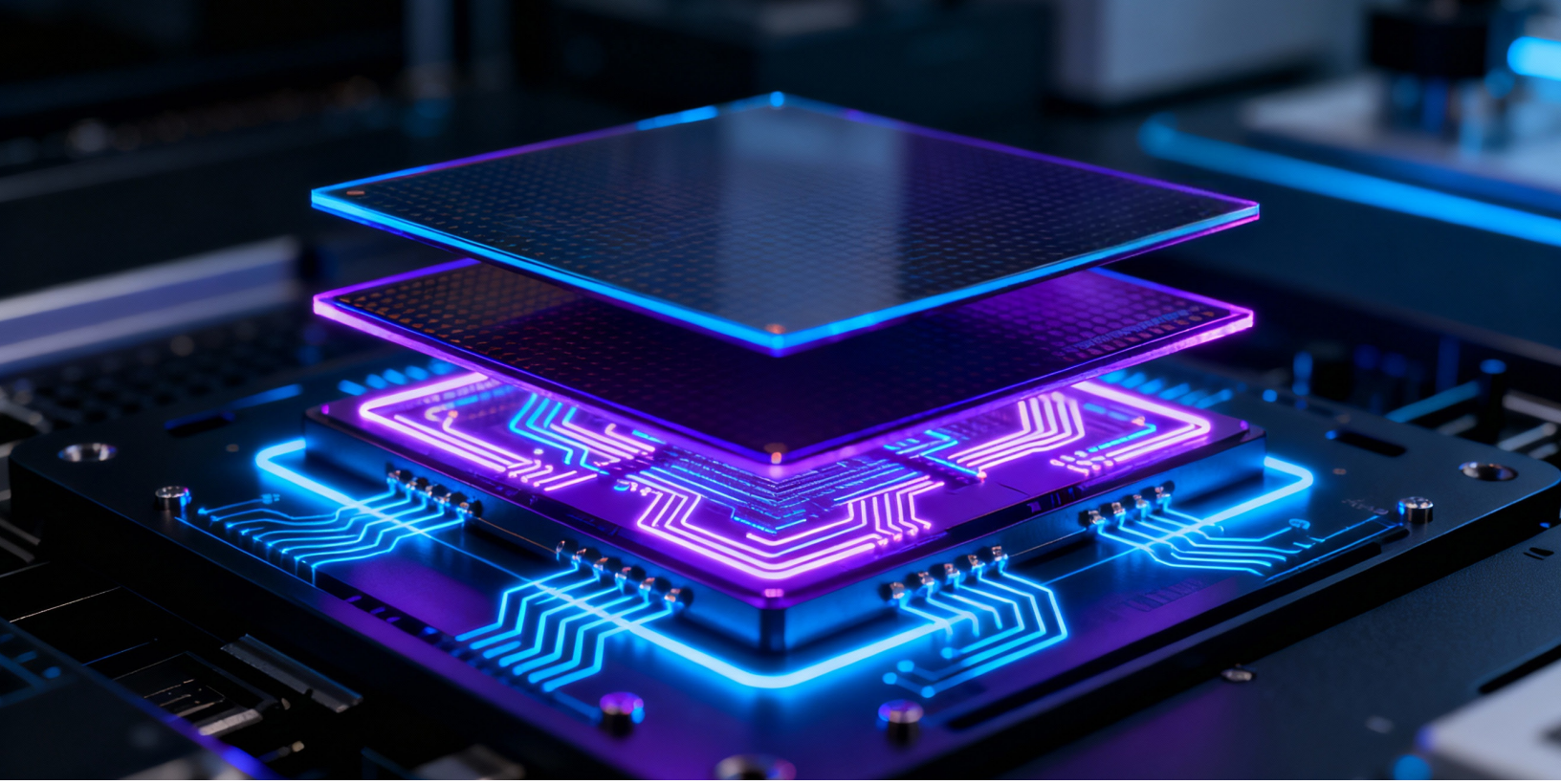
AP and HB are increasingly vital as the semiconductor industry seeks to improve performance, power, area, and cost (PPAC). With the slowdown of Moore's Law, chiplet disaggregation and 2.5D/3D integration increasingly play a key role in delivering additional PPAC gains by enabling smaller and reusable dies that improve system yield and manufacturability versus large monolithic system-on-chip (SoC). This shift is especially critical for AI and high-performance computing (HPC) workloads, where increasingly complex AI models and associated compute intensity require ultra-low latency and high-bandwidth interconnect. By shortening the interconnect paths and utilizing Cu-Cu interconnect, AP reduces energy consumption, improves latency, and lowers total system costs in comparison to large-die integration and printed circuit board (PCB)-based approaches.

Figure 1. Hybrid Bonding for High-Density Chip-to-Chip Interconnects



Source: Applied Materials

As microbump scaling is constrained at ~10–20 µm pitch, HB is essential to push beyond this limit. HB enables notable efficiency gains, driving energy below 0.05 pJ/bit, lowering latency, and supporting higher bandwidth density. Equally important, HB allows functional integration such as cache-on-logic, logic–logic tiling, and tighter logic–memory coupling with high-bandwidth memory (HBM). As HBM stacks increase in height, thermal dissipation emerges as a critical bottleneck, since the logic die at the base must dissipate more heat through increasingly resistive DRAM layers. This challenge intensifies as memory makers target 16-high and beyond with future products such as HBM4, HBM4E, and eventually HBM5. Against this backdrop, AP and HB should not be seen as incremental enhancements, but rather as foundational technologies that will define the next decade of semiconductor scaling.



Applied Materials' Role in Advanced Packaging

Applied Materials sits at the center of the industry's pivot toward AP and HB, positioning itself as a critical enabler of next-generation semiconductor scaling. This makes the ability to engineer the entire bonding stack—materials, processes, and integration—become vital. Applied's current portfolio offers an end-to-end footprint across the packaging flow, spanning dielectric stack deposition (CVD), redistribution layer etch, barrier/seed physical vapor deposition (PVD), Cu pad fill via electrochemical deposition (ECD), chemical mechanical polishing (CMP) with precise dishing control, anneal, and surface preparation. The strength of its platform lies not only in tool coverage but also in its Integrated Materials Solutions approach, where flagship systems such as Producer®, Endura®, Mustang®, and Reflexion® LK are co-optimized with advanced metrology and inspection to deliver higher yield and more predictable performance.

Applied has also built a strategic collaboration network to accelerate adoption. Its partnership with Besi anchors the integration of hybrid bonding, while its Packaging Development Centers—such as the flagship Advanced Packaging Development Center in Singapore—serve as customer co-creation hubs, enabling early learning cycles and de-risking production ramps.

This strategy gives Applied a unique advantage: control of the full-stack bonding process from materials through integration. In a domain where yield variability can quickly undermine cost and performance targets, Applied's integrated and full-stack platform mitigates risk, shortens the learning curve, and deepens customer trust. In effect, the company has positioned itself not simply as a supplier of tools, but as an indispensable partner in the shift toward chiplet architectures, 3D integration, and the high-bandwidth, low-latency systems that will define the AI and HPC era.

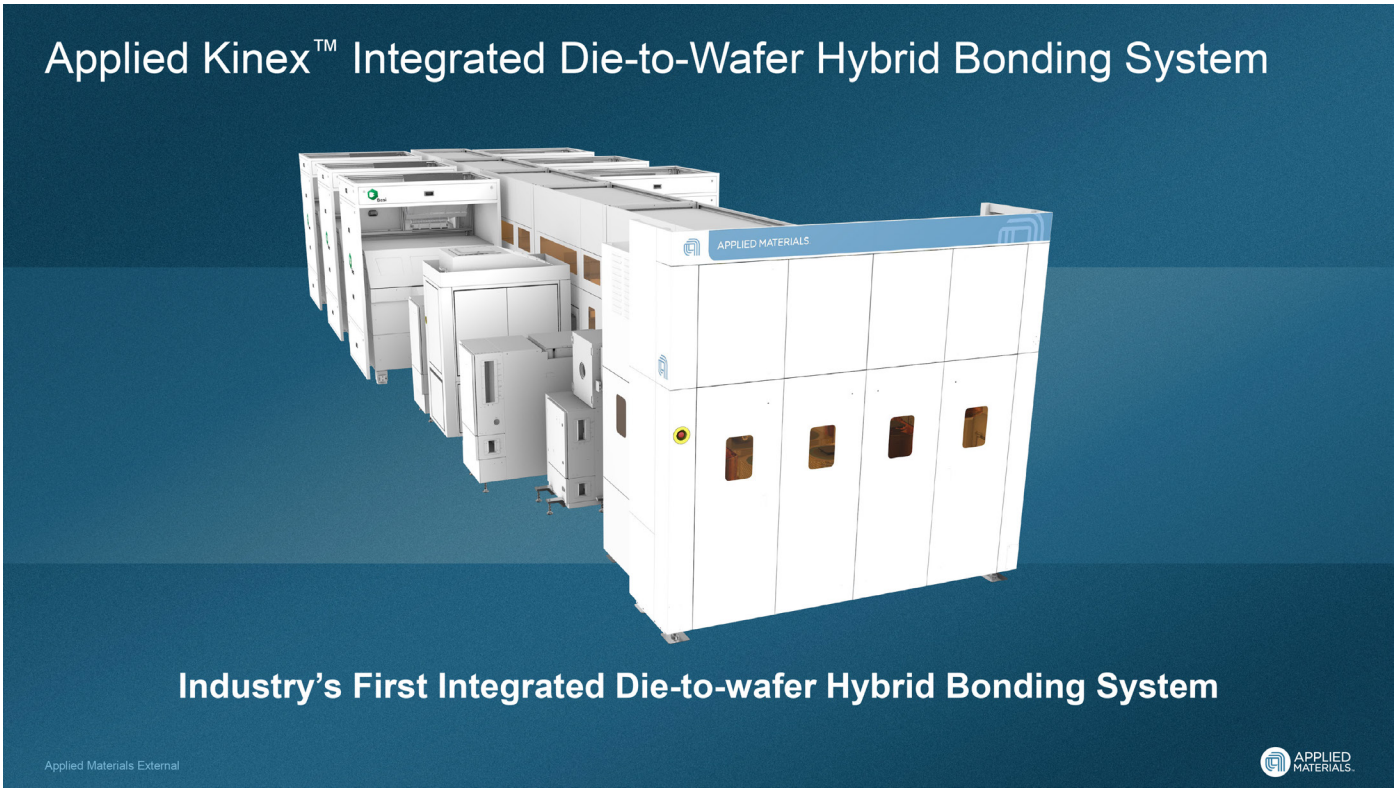
Applied Materials–Besi "All-In-One" Hybrid Bonding Solution: Kinex

Applied Materials' new **Kinex™ platform** represents the industry's first fully integrated die-to-wafer (D2W) hybrid bonding system, engineered to address the complexity of next-generation AI, HPC, and memory packaging. Unlike point-tool approaches, Kinex consolidates all critical steps—**wet clean, plasma activation, degas, IR metrology, integrated hybrid bonder, and on-tool buffer (OTB)**—into a unified platform. This ensures consistent process flow, minimizes queue-time variation, and reduces contamination risk, both of which are key determinants of bond yield.

At the core is **Besi's best-in-class hybrid bonder**, capable of ~100 nm alignment accuracy, giving Kinex the precision required for fine-pitch interconnects (<10 µm) and future HBM/logic-memory integration. The system is built on a **modular, scalable architecture**: from R&D labs with 1–2 bonders, to early/low-volume manufacturing (2–4 bonders), and finally to high-volume production configurations with up to six bonders. The system has demonstrated bonding capability for 16-high (or more) DRAM stacks, positioning it as a viable solution for the most demanding HBM configurations in next-generation AI accelerators.

Software and metrology are equally critical differentiators. The Smart Sequencer orchestrates die handling, while advanced analytics enable die traceability, predictive preventive maintenance, queue-time monitoring, and closed-loop overlay (OVL) control. This software feature ensures not only operational efficiency and accuracy but also faster learning cycles during customer ramp.

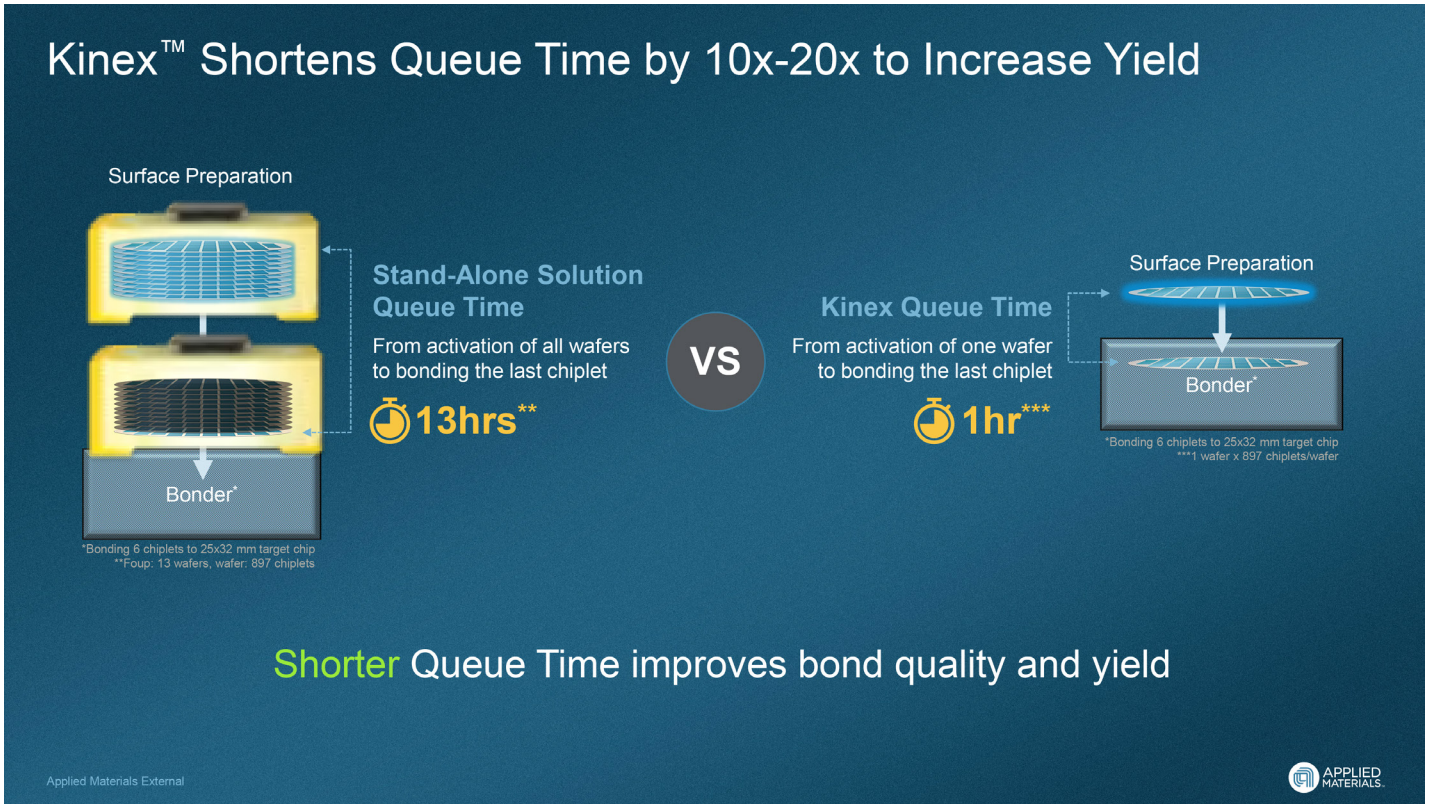
Figure 2. The Kinex™ Platform



Source: Applied Materials

The key value of Kinex lies in translating integration into measurable yield and productivity improvements. Integrated queue-time control keeps bonded surfaces chemically active, reducing void formation and safeguarding yield. This is further reinforced by stringent particle and cleanliness management, both at the tool and mini-environment level. Applied's automated OVL inspection accelerates iteration time from 1–2 hours down to ~10 minutes, a step-change in cycle-time efficiency. Meanwhile, the Class-1 mini-environment, validated with extended wafer marathon runs, demonstrates superior particle control and consistent bond yield across extended production runs.

Figure 3. Impact of Queue Time on Yield with Kinex™



Source: Applied Materials

Finally, Applied leverages its strategic collaboration with Besi: the partnership integrates Applied's process modules (CVD, PVD, ECD, CMP, surface prep) with Besi's hybrid bonder technology, while a joint field support structure ensures uptime, scalability, and maintenance services in customer fabs. The joint field support model provides comprehensive, end-to-end support for Kinex's customers ramping into high-volume manufacturing—an essential foundation for achieving the stability and consistency required in advanced, high-volume chip production.

Analyst Recommendation and Outlook

Applied Materials' Kinex system marks a critical inflection in the competitive dynamics of the hybrid bonding equipment market. By delivering the industry's first **fully integrated chiplet HB platform**, Applied is positioning itself several steps ahead of rivals. The integration of wet clean, plasma activation, degas, inline metrology, and Besi's best-in-class hybrid bonder into a single modular platform eliminates one of the largest bottlenecks in high-volume chiplet production: queue-time management. By reducing variability between process steps and embedding automated metrology at the point of bonding, Kinex directly addresses yield, throughput, and cost-of-ownership—factors that determine whether hybrid bonding can scale beyond pilots into mainstream adoption. On the technical front, we believe Applied's integrated approach to hybrid bonding sets a key precedent, signaling that other semiconductor equipment vendors are likely to follow with similar strategies, given the significant advantages brought by the integrated approach.

From a strategic standpoint, Applied has designed its product roadmap closely aligned with leading foundries and memory customers to ensure that Kinex is qualified on the most advanced programs, from cache-on-logic demonstrations to early 16-high DRAM stacking. These early collaborations validate Kinex's scalability and give Applied a first-mover advantage in securing adoption for future HPC and AI applications.

However, we see several risks. HBM adoption on hybrid bonding remains limited for now, and future uptake will depend on memory vendors' roadmaps and AI chip designers' performance targets and hardware roadmap. Hybrid bonding, in particular, remains process-sensitive—surface activation, defect density, and pad profile control all represent yield choke points that could limit scaling in the near term. Moreover, global service and support will be tested as customers attempt to move from pilot lines to multi-bonder configurations in high-volume fabs. Despite these risks, we believe the trajectory is clear. Hybrid bonding adoption is ultimately inevitable, and we expect it to become the **next battleground for chipmakers to differentiate and gain performance advantage**, particularly from the latter half of this decade onward.

Looking ahead, we see a staged adoption curve. In the 2027–29 period, we expect gradual penetration into chiplet-based CPUs, GPUs, and XPUs, alongside pilot HBM programs as DRAM makers explore hybrid bonding for next-generation stacking, which we anticipate to happen around HBM4E 16hi or HBM5. By the end of the decade, hybrid bonding could become the mainstream path for high-capacity HBM, logic-memory hybrids, and emerging areas such as co-packaged optics. If Applied and Kinex can sustain its technical lead, Applied stands to capture a disproportionate share of this incremental TAM of AP and HB—a market we firmly believe has a lot of upside, given the technology trend we are seeing.

Challenges such as queue-time management and nanometer-scale defect control remain, but we expect Applied, together with Besi and leading memory and foundry partners, to address these through joint development and process co-optimization. We view hybrid bonding not as a niche, but as the critical interconnect for a future driven by chiplets, HBM, and AP. With Kinex, Applied has positioned itself at the center of this transition, and we believe the long-term growth opportunity supports a constructive outlook and potential share gains versus peers.

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