Implant Applications for Emerging Logic Technologies

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Outline

- FinFET Challenges
- Doping Requirements
- Implant Solutions
  - Crystal Damage Engineering
  - Hard Mask
  - Transistor Tuning
FinFET Processing Challenges
an Ion Implantation Perspective

Doping
- Fin Junctions
  - Rext, leakage, overlap, SCE
  - Uniform fin doping
  - Fin damage control
  - Diffusion control
  - Contact Rc reduction
  - New materials (Ge/III-V)

Precision Material Modification (PMM)
- Gate Stack
  - Vt tuning
  - Work function tuning

PMM
- Fin Height Control
  - Pattern loading
  - STI Oxide Etch back

PMM
- Spacer
  - Spacer Etch – selective spacer removal from Fin
# FinFET Challenges – an Implant Perspective

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FinFET Front End Process Flow - Example

- Undoped Epi - option
- Fin Patterning
- Ground Plane/ Well Implant formation
- Well Anneal
- STI Oxide Etchback  ESL
- Dummy Gate Patterning
- Halo/SDE Formation  (Dopant/ co implant/thermal)
- Anneal
- ESD/ stressor
- Top off SD implant
- Anneal
- Silicidation
- Replacement Metal Gate

**FinFETs require several implant steps for device performance and minimizing device variability**
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Ion Implantation Technologies for Advanced Logic

Damage Engineering & New Species

Applications

- SDE/SD/contact/Halo/Vt/ Well
- Work function tuning

Key features:

- Implant dose and depth control
- Wide range dose/ energy
- Adjustable implant angle
- Wide range of implant species
- Damage Engineering
Hot Implant Maintains Crystalline Fin

Hot implant enables thin Fin: eliminates amorphization during implant, reduces defects after anneal.
Hot Implant Benefit

*Fin Diodes and Resistors*

**Lower Damage**

- Lower junction leakage

- Hot implant + Spike

- RT implant + Spike

**Better Dopant Activation**

- Improved small CD conductance

- 5X

- Hot implant + Spike

- RT implant + Spike

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**Graphs:**

1. **Lower junction leakage**
   - Log10 Diode Junction leakage at 5V (A) low
   - CD

2. **Improved small CD conductance**
   - Fin Line Conductance (1/ohms)
   - Wfin (nm)
Hot Implant: Predictable Defects & Dopant Profiles

TCAD predicts trends for (a) defects, (b) activation and (c) dopant profiles for hot implants

Arsenic Clusters Count in Fin
1000°C spike

Less clusters → Better Activation!

TCAD predicts trends for (a) defects, (b) activation and (c) dopant profiles for hot implants
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Hard Mask Requirements for Hot Implant

1. Deposition (coverage)
2. Patterning (no fin damage)
3. Remove PR (no fin damage)
4. Hot Implant (block)
5. HM removal (selectivity)

Hard mask requirements:
1. Good coverage
2. Block hot implant
3. Removable
4. No fin damage
Hard Mask Enables More Sidewall Doping

Hard mask allows higher implant angles for the sidewall.

<table>
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<tr>
<th>Mask</th>
<th>Mask Thickness</th>
<th>Maximum Tilt Angle for Doping Fin Sidewall Adjacent to Mask</th>
<th>Active Arsenic Concentration at Fin Sidewalls at Mid-Fin Height</th>
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<tbody>
<tr>
<td>Photoresist</td>
<td>200 nm</td>
<td>6°</td>
<td>$5 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Hard Mask</td>
<td>40 nm</td>
<td>21°</td>
<td>$1.4 \times 10^{20}$ cm$^{-3}$</td>
</tr>
</tbody>
</table>

After 1025°C 0.5 sec anneal

- Photoresist 200 nm, Tilt = 6°
  - Active Arsenic Concentration (AsActive) [cm$^{-3}$]:
    - Width 14nm, height 28nm, pitch 60nm

- Hard Mask 40 nm, Tilt = 21°
  - Active Arsenic Concentration (AsActive) [cm$^{-3}$]:
    - Width 14nm, height 28nm, pitch 60nm
Hard Mask: Strippable Conformal Carbon

Key Differentiation:
- 100% step coverage on both isolated and dense structures
- Wide temperature window: <100-550°C
- Conformal/Gap filling
- Zero micro-loading
- Easily strippable in O₂ plasma or non-O₂ plasma

Applications:
- FEOL: Hot implant hard mask; Gate cut/ gate contact CD shrink
- BEOL: Via CD shrink; Spacer double/triple/ quad patterning

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<th>Parameters</th>
<th>Properties</th>
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<tr>
<td>Deposition Temperature</td>
<td>&lt;100-550°C</td>
</tr>
<tr>
<td>Step Coverage - Open / Dense</td>
<td>100% / 100%</td>
</tr>
<tr>
<td>Sidewall Microloading</td>
<td>~0%</td>
</tr>
<tr>
<td>Stress</td>
<td>&lt;50MPa (Tensile)</td>
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Conformal Carbon Film Overcomes the Topography Challenge in Advanced Patterning
## Carbon Hard Mask Strip: XPS Data Post Implant

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<th>Parameters</th>
<th>Performance</th>
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<tbody>
<tr>
<td>Implant temp (°C)</td>
<td>hot</td>
</tr>
<tr>
<td>Implant species</td>
<td>No implant</td>
</tr>
<tr>
<td>Implant condition</td>
<td>No implant</td>
</tr>
<tr>
<td>% Shrinkage</td>
<td>2% (thermal shrinkage at 450°C 10min anneal)</td>
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<td>Implant temp (°C)</td>
<td>hot</td>
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<tr>
<td>Implant species</td>
<td>BF2 implant</td>
</tr>
<tr>
<td>Implant condition</td>
<td>10keV, 1e15</td>
</tr>
<tr>
<td>% Shrinkage</td>
<td>5%</td>
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<td>As implant</td>
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<td>% Shrinkage</td>
<td>6%</td>
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### Post strip data with non-O2 ash at 150C

- XPS data, B: not detected
- XPS data, As: not detected

**Carbon hard mask blocks implant effectively**
Other Hot Implant Applications for FinFET
Benefits for S/D and Strain

**Low Dose Deep SD**

- Graded profile (less E-field leakage)
- Hot implant improves process margin / epi film quality
- Reduce defectivity (lower leakage)

**Top off Deep SD**

- Increase activation (lower Rc)
- Hot implant reduces strain relaxation in SiGe/ SiCP (higher mobility)
- Reduce defectivity (lower Leakage)

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*Ph 20kV 4.5e13, 1000C anneal*

Defects

No Defects
Hot implant for Vt/Well/GP

Reduced diffusivity and defectivity for improved process margin / variability

Hot implant: More abrupt/shallower profile with reduced defectivity
Hot Implant: Extendable Technology

Lower Damage on III-V

Hot Si Implant  RT Si Implant

InGaAs

High Dose / Low Damage Implant for InGaAs

Lower Damage on Ge

Boron Hot Implant

- Unimplanted controls
- B11 at 5.5e14
- B11 at 2.2e15
- B11 at 1.1e16

Applied / IITB Data

Higher Temperature Recovers Raman Intensity

Hot Implant Extendable to New Channel Materials
Outline

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## FinFET Precision Material Modification

### Examples

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<th>Applications</th>
<th>Solutions</th>
<th>Advantages</th>
<th>Results</th>
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<td>Metal Salicide (Contact Resistance)</td>
<td>SBH (Rc)</td>
<td>Al, S, Se</td>
<td>Reduce Rc</td>
<td>SBH: &gt; 60% Rc reduction by post-Se I/I with TiSi$_2$ and CoSi$_2$ on TLM structures</td>
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<td>Metal Gate (Multi-$V_{th}$)</td>
<td>eWF Tuning</td>
<td>F, Ge, Al, O, N (C, Si)</td>
<td>Tunability</td>
<td>N, F imp demonstrated for DMG: +200mV by N into TiAl, +80mV by F into TiN om MOSCAP</td>
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<td>Fin Height Control</td>
<td>STI Oxide Recess PLE Reduction</td>
<td>ESL by Si IMP</td>
<td>Reduce etch loading effect</td>
<td>Si imp reduces oxide E/R by 2X blanket</td>
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## Summary

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