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Nickel silicide formation using low-temperature spike anneal

OVERVIEW

The manufacture and future development of integrated circuits and devices face many technological challenges, some of which are materials-related, while others are related to process integration. This work presents an example of the extendibility of rapid thermal processing (RTP) in a transistor manufacturing environment over a temperature regime that addresses sub-300°C processing requirements.

Nickel silicide (NiSi) is emerging as the choice material for contact applications in semiconductor device processing for the 65nm technology node and beyond. The Ni/Si solid-state reaction has been widely studied in recent years [1, 2], with several papers presented at recent IEDM conferences that highlight the merits of NiSi for shrinking device geometry, strained silicon in the channel [3], use in poly silicon-germanium, and use in dual metal-gate technology development [4].

The overall integration of NiSi as the contact material in CMOS process flow is influenced by variables that include the substrate, metal

deposition [6], ion implantation [7], and gate dielectric parameters. The two-step annealing sequence is common in the industry for Co and Ti silicide applications, and incorporates a wet removal of unreacted metal film after the silicide formation. In the case of Ni, the possibility of forming the mono-silicide phase in one step is under consid-

eration. Since Ni is the diffusing element in the reaction, however, the one-step anneal process may result in excessive silicidation on the polysilicon layer of the gate stack [5, 6].

Phase transformation during the silicide reaction is commonly characterized by measuring the sheet resistance (R_s in $\Omega/\text{sq.}$) of the metal film as a function of processing temperature. Figure 1 shows data from silicon wafers deposited with 10nm Ni (with a 10nm TiN cap layer) for three different dwell times (0, 30, and 60 sec soak at the highest temperature). With an increase in temperature, the solid-state reaction between Ni and Si progresses from the nickel-rich (Ni_2Si) to the silicon-rich (NiSi_2) silicide phase. The desired phase is the monosilicide (NiSi) that has the lowest R_s value (typically in the 350–550°C range). For the long soak processes, the transformation to NiSi occurs at a lower temperature. This behavior is expected in accordance with a predominantly kinetics-driven reaction mechanism [8].

Low-temperature spike anneal

Since diffusion kinetics is suppressed for the shorter anneal process and Ni is the diffusing species in the NiSi reaction, there are many motivations for reducing the thermal budget of the silicidation process. Spike anneal has been shown to reduce the reverse linewidth effect (decreasing R_s with shrinking gate length) — a problem caused by uncontrolled and undesirable diffusion of Ni into the Si at the corners of active areas such as the isolation and spacer regions [6, 9].

Another challenge with the integration of NiSi is an increase in the junction leakage current due to the presence of a rough interface between NiSi and Si. Spike anneal offers the ability to limit diffusion, thereby controlling the silicide-silicon interface morphology. It becomes increasingly critical to control silicon consumption as the junctions get shallower with technologies scaled at 45nm and beyond. As fully silicided gates are now being investigated as alternatives to metal gates, control of Ni diffusion in the (doped)

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polysilicon is critical to reap the benefits of work-function modifications while preventing Ni from diffusing into the gate oxide [10].

Thermal stability of NiSi is potentially the biggest factor that will determine the annealing solution for silicide formation [11]. The morphology and crystallography of the Ni₂Si phase may influence the thermal stability of the NiSi phase. Altering the thermal stability of NiSi is also possible by alloying [5, 12, 13] and implantation techniques [7]. Previous work documented interesting crystallographic orientation changes (of the Ni₂Si phase) as a function of peak temperature; the low energy (002) orientation is observed at the higher anneal temperature [14]. Orientation of Ni₂Si will likely influence the crystallographic relationship of the NiSi phase with the underlying Si (after the second RTP step).

Since NiSi (orthorhombic crystal structure) exhibits a rare negative expansion coefficient along one of the axes, it has unique thermal implications in a thin-film form. Therefore, it is anticipated that the stress effects on the NiSi film will be altered as a function of temperature and dictated by the crystallographic orientation of NiSi with the substrate [15]. Grain texturing is expected to play a role in the agglomeration (de-wetting) behavior of NiSi at elevated temperatures (>500°C). Consequently, it is critical to control the thermal budget of the devices during and after NiSi processing as compared to its predecessor contact materials (Co- and Ti-based silicides).

Spike anneal is increasingly being used for the silicidation process. This anneal is similar to the fast ramp-up and ramp-down in temperature used for implanted dopant activation, which is now a common RTP application for ultrashallow junction formation. An example of spike anneal trace is shown in Fig. 2. The “0 second” spike is named to represent a virtual “no soak” condition at the highest temperature. Uniform temperature control across the wafer during ramp-up and ramp-down portions of the anneal process is evident from the trace in Fig. 2. Traces T1 through T7 represent the temperature recorded at different radial locations on the backside of the wafer (300mm dia.).

Advances in RTP technology

One of the challenges of processing wafers at low temperatures in a lamp-based RTP chamber is the ability to collect adequate signal in the wavelengths of interest (near infrared). At these temperatures (<400°C), the thermal emission from the wafer, collected by the pyrometer, is affected by the light transmitted through the process kit/gap between the edge ring and wafer, which can result in inaccurate interpretation of the wafer temperature.

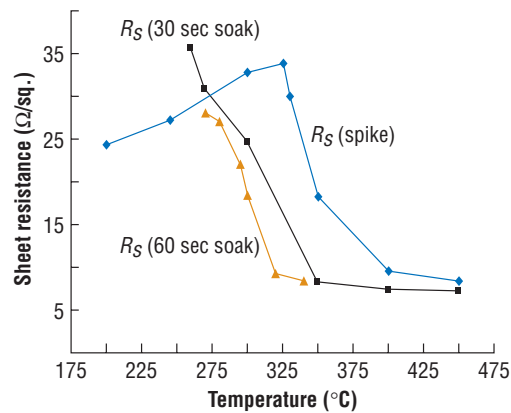


Figure 1. Phase transformation characteristics of a 10nm Ni film (with TiN cap layer) for three different dwell times (at the highest temperature): 0, 30, and 60 sec.

this work, a real-time temperature measurement capability over a wide range of temperatures (50–1300°C) has been accomplished. Figure 3 shows that a wafer temperature well below 250°C was recorded using proprietary temperature-measurement technology.

Process monitoring

Chamber performance monitoring is an essential ingredient to process monitoring. During the transformation from Ni₂Si to NiSi, the R_s value decreases rapidly for a small change in temperature (Fig. 1). Sensitivity to R_s as a function of temperature is commonly used to monitor the stability of the anneal process. The temperature nonuniformity therefore is best quantifiable at the point of inflection in the transformation curve, where a mixture of the Ni-rich and monosilicide phases are present. The steepest portion of the transformation curve serves well as a metric to estimate the robustness of temperature control over a period of time, as well as an indicator of the repeatability of temperature-uniformity performance across the wafer.

The pre-anneal condition of the wafer should be stable and consistent to reliably evaluate the stability of the annealing system. For the reported repeatability tests, the substrates (300mm P-wafers) were cleaned (in a diluted HF, 100:1 solution) to remove native

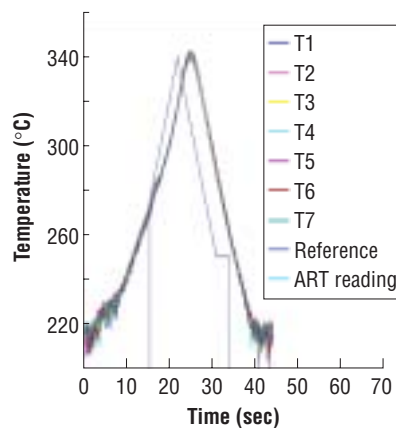


Figure 2. Time-temperature profile for a 340°C spike anneal process on a 300mm wafer. The traces labeled T1–T7 represent the pyrometer readings that record the wafer temperature at various radial locations.

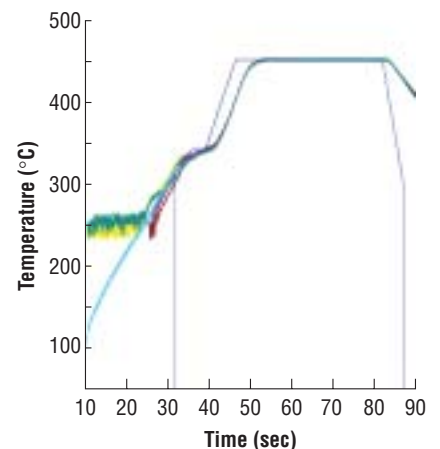


Figure 3. A time-temperature profile on a 300mm wafer demonstrates the extendibility of the temperature measurement to <100°C using proprietary technology.

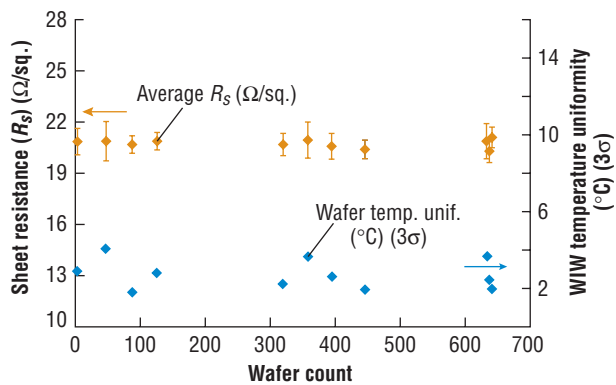


Figure 4. Repeatability of the spike process is demonstrated over a 700-wafer period. The overall temperature uniformity is $<3^{\circ}\text{C}$ (3σ).

oxide. Within 24 hrs following the clean, the wafers were loaded onto an Applied Endura physical vapor deposition (PVD) system. The wafers were then sputter-cleaned with argon prior to depositing 10nm of Ni; following the Ni deposition, a 10nm TiN layer was deposited.

Using the R_s vs. temperature data for the spike process shown in Fig. 1, it was determined that a 340°C spike anneal condition (targeting an R_s value of about $20\Omega/\text{sq.}$) would be the ideal temperature monitor to test the stability and performance of the RTP chamber. Temperature monitors were processed periodically during a continuous cycle of more than 700 wafers.

After anneal, R_s was measured on the wafers using the four-point probe technique. A total of 121 points was collected from each monitor wafer (with an exclusion of 3mm from the wafer edge); the results are shown in Fig. 4. The trending of R_s value on each monitor is plotted on the y axis in this chart; the secondary y axis represents the temperature equivalent of the nonuniformity (in $^{\circ}\text{C}$, 3σ) within each wafer. This value is $>4^{\circ}\text{C}$ (3σ). Cumulative temperature nonuniformity of all the data points (11 monitor wafers, 121 points/wafer, or 1331 points total) over the 700-wafer processing period is $<3^{\circ}\text{C}$ (3σ). The repeatability of the peak temperature was $<0.5^{\circ}\text{C}$ over this processing period. System performance at this level of repeatability will meet the production-worthy requirements for processing the next several generations of devices.

Conclusion

Lamp-based RTP technology has been improved to process wafers at low temperatures ($<400^{\circ}\text{C}$) that were previously challenging. Specifically, low-temperature spike anneal is a strong candidate for NiSi processing as evidenced by the following:

- 1) For a typical Ni film thickness ($\sim 10\text{nm}$), the onset of NiSi formation can be delayed by $\sim 50^{\circ}\text{C}$ using a spike process when compared to a 30 sec soak anneal process ($>70^{\circ}\text{C}$ when compared to a 60 sec soak process).
- 2) Process performance monitoring for a 340°C spike process has been demonstrated. Temperature control and repeatability within 3°C (3σ) meets production requirements for 300mm wafer processing.

bility within 3°C (3σ) meets production requirements for 300mm wafer processing.

In addition to delineating the temperature effects of silicide formation, low-temperature processing capability will be useful for critical processes such as annealing high- k thin films and some backend anneal applications for future devices.

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