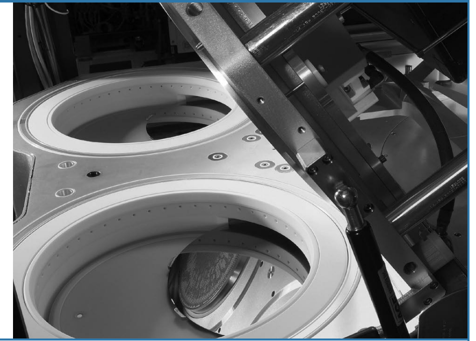
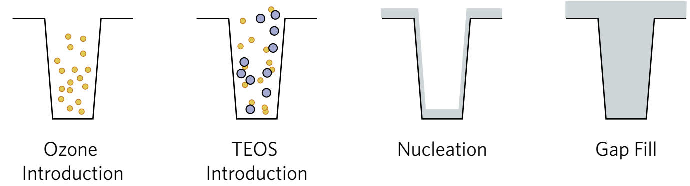
APPLIED PRODUCER® HARP™

Advanced STI and PMD Gap Fill for ≤65nm Technology Nodes

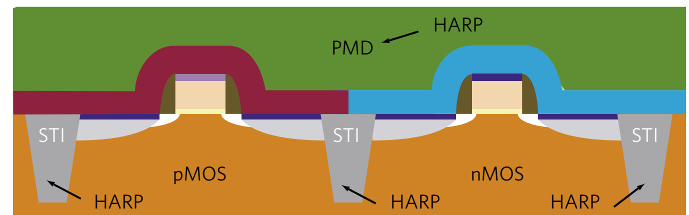


Rapid progress in transistor scaling has made void-free, high aspect ratio gap fill increasingly challenging. Applied Producer HARP (High Aspect Ratio Process) is a thermal CVD (Chemical Vapor Deposition) gap fill solution that addresses the stringent ≤65nm/70nm Logic and Memory requirements for shallow trench isolation (STI) and pre-metal dielectric (PMD) applications, with extendibility to the 45nm/55nm nodes and beyond. Using patented TEOS (tetraethyl orthosilicate)/ozone chemistry, the HARP technology delivers void-free high aspect ratio gap fill with strain engineering capability for improved electrical performance. HARP successfully fills 24nm STI features with >10:1 A/R and 10nm PMD features with >8:1 A/R, while improving isolation performance and enhancing nMOS and pMOS transistor performance. Applied Producer HARP is used in production for 65nm Logic and 70nm Memory, and is qualified for 45nm Logic and 55nm Memory.

HARP PROCESS SEQUENCE



HARP APPLICATIONS



HARP ROADMAP (Logic/Memory)

90nm	65nm/70nm	45nm/55nm
Ultima X™	Ultima X HARP	Ultima X HARP

FEATURES

- Thermal process eliminates plasma damage
- Lower metal contamination compared to conventional plasma processes
- Induces tensile stress into silicon
- Patented TEOS/ozone chemistry for conformal fill
- Production-proven Producer platform with >500 SACVD systems worldwide

BENEFITS

- Void-free high aspect ratio gap fill (STI: 24nm feature size, >10:1 A/R; PMD: 10nm feature size, 8:1 A/R)
- Meets low thermal budget required for Flash and NiSi integration
- Proven CMP integration with low cost of ownership
- Enables higher transistor drive current for increased transistor speed
- Reduced gate leakage and improved retention for Flash
- Improved device reliability

APPLIED MATERIALS®

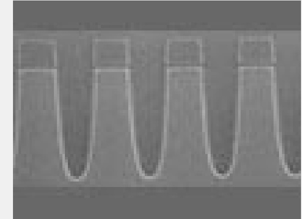
With its thermal (non-plasma) CVD process, HARP eliminates plasma damage to the wafer, enabling improved device reliability. The technology delivers a >20% improvement in breakdown voltage over standard processes with equivalent device yield. HARP also provides lower metal contamination compared to conventional plasma processes.

In addition to gap fill applications, HARP plays a key role in strain engineering at the STI and PMD levels to enhance transistor speed. HARP features a unique ability to enhance transistor performance by depositing stress-inducing films which enable a significant increase in drive current with no additional cost or mask layers. These gains in speed can account for >20% of the total transistor speed improvement required per chip generation without added integration complexity. Maximum performance gain is achieved by using HARP for both STI and PMD fill. When used independently, HARP STI and HARP PMD enable >10% and 6% increased nMOS drive current, respectively, for 65nm devices.

For non-volatile memory (NVM) technologies such as Flash, the strained HARP film reduces leakage current to improve charge storage and retention. In addition to the leakage benefit, strain introduced in the NVM cell improves drive current for faster read times, pushing out the scaling limits of conventional floating gate flash technology.

The HARP process runs on the production-proven, high-throughput Producer system. Platform extendibility allows customers to leverage the same Producer toolset for multiple device generations. For integration, CMP (Chemical Mechanical Planarization) processes have been developed for the HARP post-deposition topography. This proven CMP integration is achieved without adding complexity to the process flow, resulting in lower cost of ownership.

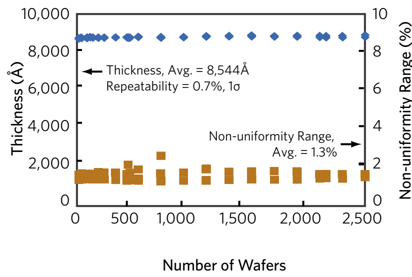
HARP Gap Fill
65nm node, >6:1 A/R



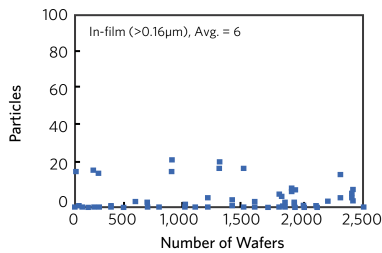
HARP DEMONSTRATED PERFORMANCE

HARP STI

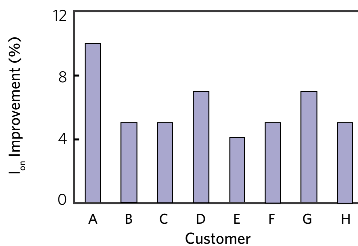
Thickness Repeatability



Particle Performance

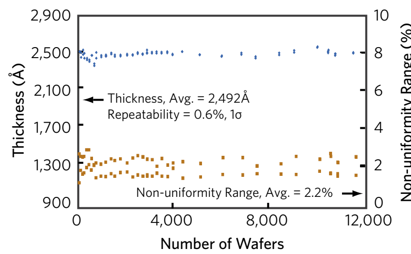


I_{on} Improvement

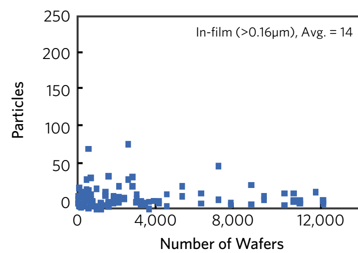


HARP PMD

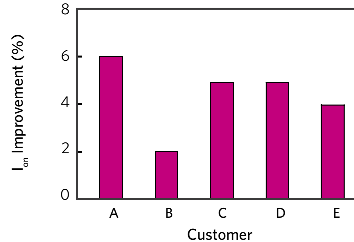
Thickness Repeatability



Particle Performance

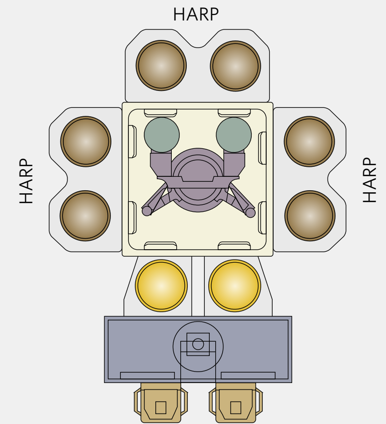


I_{on} Improvement



BKM CONFIGURATION

300mm Producer HARP



Throughput >60wph (PMD)

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