Fabrication and Electrical Characterization of 5×50um Through Silicon Vias for 3D Integration

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Abstract

We present fabrication, electrical characterization, and metrology analysis results of 5×50um TSVs for 3D integration. Specifically, electrical performance of blind TSVs is evaluated by capacitance-voltage (CV) and current-voltage (IV) measurements. Important electrical parameters such as oxide capacitance, minimum TSV capacitance, leakage current, and breakdown voltage are extracted and show good results. The capacitance values also closely match model predictions. The electrical testing data are further verified with a variety of materials analysis techniques.

INTRODUCTION

After decades of conceiving "integrated circuits" in two dimensions, the industry is extending integration to the third dimension with through-silicon via (TSV) technology. Having progressed from developing the fabrication processes and equipment for creating TSVs (deep silicon etch, for example), through the critical phase of combining the process steps into a fabrication flow, we arrived at the point of electrically characterizing those structures to determine their functional suitability. The resulting capacitance, leakage, and breakdown measurements give confidence that the necessary elements are in place for 3D integration to succeed. 3D integration with TSVs is an advance in microelectronic packaging that is poised to transform the semiconductor industry. By connecting multiple chips in a stack with signal, power, and ground pathways running vertically through one or more of the silicon strata, the following benefits can be realized: 1) high-bandwidth, low-loss interconnection from chip to chip [1]; 2) economy of space in comparison to wire bonding, package-on-package, and other packaging schemes [2]; 3) relief from dependency on 2D scaling to achieve integration gains [3]; and 4) freedom to integrate different functions (memory, logic, etc.) supplied from different technology nodes and wafer sizes [4]. In addition to true 3D stacks, a related "2.5D" architecture is currently being adopted, where chips are stacked side by side on a silicon interposer with high-density interconnects and TSVs that lead to flip-chip connections below.

In both the 3D and 2.5D architectures, the central element is the TSV itself, whose fabrication is subject to many unit-process and process-integration challenges [5]. The primary steps in forming the via are deep silicon etch, chemical vapor deposition (CVD) of an insulating oxide liner, physical vapor deposition (PVD) of a metal barrier and seed layer, electrochemical deposition (ECD) of copper to fill the via hole, and chemical-mechanical planarization (CMP). Much of the difficulty arises from the high aspect ratio of the vias: they need to be deep to traverse the entire thickness of the silicon, and their diameters need to be small to avoid occupying valuable wafer space or affecting the performance of adjacent transistors. Advances in these unit processes and their integration have been described earlier [6].

Several key TSV functional attributes can be evaluated electrically at the wafer level [7]. In a 3D or 2.5D stack, it is important for the capacitance of the TSV to be low so that little power is lost to capacitive charging and little cross talk occurs between neighboring TSVs. It is likewise vitally important for the leakage current from the TSV to the silicon body to be low. Finally, the breakdown voltage (Vbd) of the oxide must be sufficiently high for the device to perform reliably with a long service life. Here we report on electrical characterization of TSVs that were fabricated in Applied Materials laboratories.

TSV TEST STRUCTURE AND METHODOLOGY

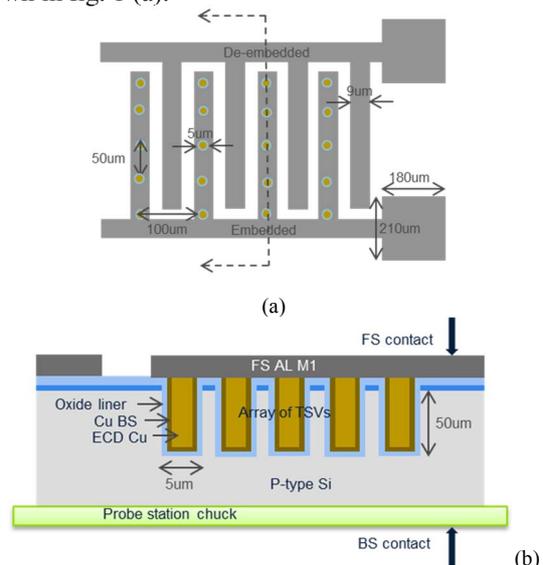We have embedded and de-embedded electrical test structures as shown in fig. 1 (a).

(a)

(b)

Fig.1. TSV electrical test structures (a) top view (b) cross-section view

Embedded structure has an array of TSVs connected to M1 on top and de-embedded structure is a pure M1 with no TSVs. Front side aluminum metal1 (FS Al M1) acts as a front side contact and back side contact is taken from chuck of probe station. We did capacitance-voltage (CV) and current-voltage (IV) measurements on embedded and de-embedded structures to characterize TSV. CV measurement is done at a voltage bias from -20V to 20V in step of 0.25V using two different techniques, quasi-static CV (QSCV) and impedance technique [8]. In an impedance technique a voltage bias and a small (30mV) alternating current (AC) signal was applied at six different frequencies 9kHz, 11kHz, 90kHz, 110kHz, 900kHz and 1MHz to measure CV using Cp-G mode. The CV data measured by Cp-G mode was corrected using four element model to eliminate frequency dispersion caused by parasitics [8]. From CV curve we can extract oxide capacitance (C^{oxide}) and minimum capacitance (C^{min}). Capacitance of one TSV was obtained by subtracting the capacitance of de-embedded structure from embedded structure followed by division with the number of TSVs (*n*). IV measurement was done in a voltage range of -100V to 100V in step of 1V. We can extract breakdown voltage from IV data.

For a blind TSV, total capacitance is a summation of TSV sidewall and TSV bottom capacitances. Theoretically, blind TSV oxide capacitance (C_{TSV}^{oxide}) and minimum TSV capacitance (C_{TSV}^{min}) can be expressed as [9], [10]

$$C_{TSV}^{oxide} = \frac{2\pi\varepsilon_{ox}L_{TSV}}{\ln\left(\frac{1}{1-\frac{2t_{ox}^{SW}}{CD_{TSV}}}\right)} + \frac{\varepsilon_{ox}A}{t_{ox}^{bottom}} \quad (3)$$

$$C_{S}^{min-dep} = \frac{2\pi\varepsilon_{si}L_{TSV}}{\ln\left(\frac{2R_{max}}{CD_{TSV}}\right)} + \frac{\varepsilon_{si}A}{\sqrt{\frac{4\varepsilon_{si}}{qN_a}\left(\frac{KT}{q}\right)\ln\left(\frac{N_a}{n_i}\right)}} \quad (4)$$

$$C_{TSV}^{min} = \frac{C_{TSV}^{oxide}C_{S}^{min-dep}}{C_{TSV}^{oxide}+C_{S}^{min-dep}} \quad (5)$$

$$\frac{qN_aR_{ox}^2}{4\varepsilon_{si}} - \frac{qN_aR_{max}^2}{2\varepsilon_{si}}\ln(R_{ox}) + \frac{qN_aR_{max}^2}{4\varepsilon_{si}}(2\ln(R_{max})-1) - 2\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) = 0 \quad (6)$$

Where ε_{ox} and ε_{Si} are electrical permittivity of oxide and silicon, L_{TSV} is a length of TSV, t_{ox}^{sw} is an average TSV sidewall oxide thickness, CD_{TSV} is a diameter of TSV, A is an area of TSV bottom, t_{ox}^{bottom} is TSV bottom oxide thickness, q is an electronic charge, N_a is a substrate doping, K is a Boltzmann constant, T is a temperature, R_{ox} is a radius of TSV, n_i is an intrinsic carrier concentration of Si and R_{max} is a maximum depletion radius which can be obtained by solving (6).

FABRICATION OF TSV TEST STRUCTURE

TSVs were formed in a lightly p-doped silicon wafers with a doping concentration in the range 10^{15} to 10^{16} cm^{-3}. Before TSV patterning, 2kÅ of CVD oxide was deposited to simulate the pre-metal dielectric layer on a device wafer (fig.2 (a)). Vias of 5μm in diameter and 50μm deep were created using the Bosch etch method in a unique inductively-coupled plasma etch chamber (fig.2 (b)). The oxide liner was deposited using a proprietary ozone/TEOS-based CVD process with highly conformal step coverage (fig. 2 (c)). It helps to provide a

smooth TSV sidewall. Liner oxide thickness as deposited was an average 250 nm on the sidewall. The PVD copper barrier tantalum (Ta) and seed (Cu BS) were deposited and the barrier has an approximate thickness of 50Å at the thinnest point (fig. 2(d)).
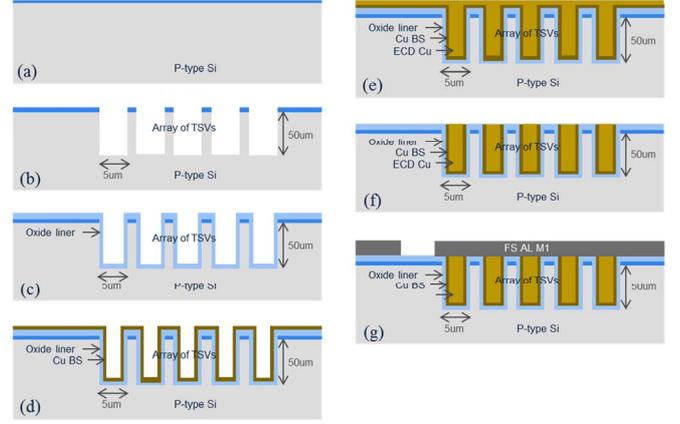

Fig. 2. TSV test structure process flow

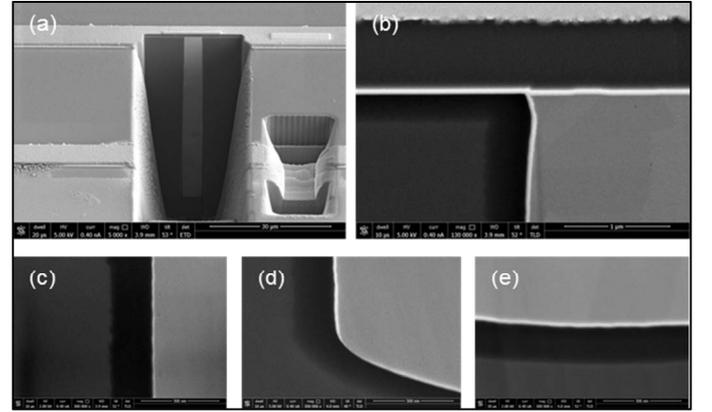Fig. 3. FIB images of a fabricated 5×50μm TSV: (a) overall TSV structure, (b) TSV top sidewall oxide, (c) TSV mid sidewall oxide, (d) TSV bottom sidewall oxide, and (e) TSV bottom oxide.

The vias were filled by copper electro-chemical deposition (ECD) in a chamber with special agitation and field-shaping features, using a programmed controlled-current waveform (fig. 2(e)). After plating, the wafer was annealed at 400°C for 30 minutes in forming gas. CMP was performed by a three-platen sequence with endpoint control. The resulting total thickness of oxide on the field was 320nm (a combination of the blanket HDP oxide and the TSV liner oxide that remained after CMP) (fig. 2(f)). A front side metal1 (FS M1) comb pattern was made by PVD and etches of aluminum traces 9μm wide above the copper TSVs, leading to 210×180μm probe pads (fig. 2(g)). The fabricated TSV is shown in fig. 3 (a) and field, mid sidewall, bottom sidewall and bottom oxide are shown in fig. 3 (b)-(e).

ELECTRICAL CHARACTERIZATION OF TSVs

We did electrical testing (CV and IV measurements) on embedded and de-embedded structure. Embedded structure has 240 TSVs with a pitch of 50Y100X and M1 on top. De-embedded is a pure M1 structure. From CV and IV

measurement data of embedded and de-embedded structures, we extracted capacitance and leakage of one TSV as shown in fig. 4 and 5. The oxide capacitance measured by QSCV and impedance techniques are pretty similar and reasonably matching with the model prediction as can been seen in Table1. Also, the minimum TSV capacitance shows a close match with the model. The leakage current of one TSV is less than 1×10^{-13}A with no TSV breakdown in a wide range of voltage from -100 to 100V as shown in fig. 5 and Table1.
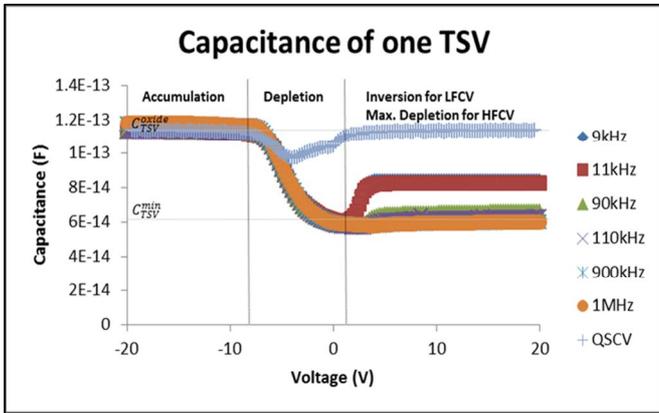
Fig. 4. Capacitance of one TSV obtained from CV of embedded (240 TSVs with M1 on top) and de-embedded (pure M1) structures using quasistatic and impedance technique at different frequencies
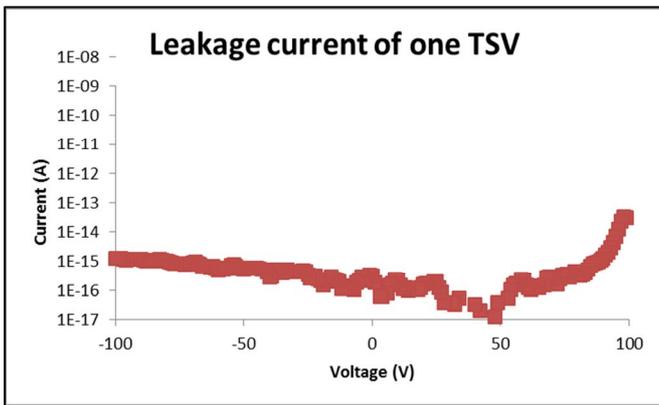

Fig. 5. Leakage current of one TSV obtained from IV of embedded and de-embedded structures

Table1. Experimental vs. model results of one TSV

Parameters	Experimental	Model/Theory
C_{TSV}^{oxide}	117fF	108fF
C_{TSV}^{min}	61fF	57fF
I_{leak}	$<1 \times 10^{-13}$ A	NA
V_{bd}	No breakdown from -100V to 100V	8MV/cm or 200V (for 250nm thick oxide)

To verify the oxide-substrate and barrier-oxide interface integrity, we performed materials metrology analysis on our wafers, including high angle annular dark field (HAADF) imaging, transmission electron microscopy (TEM), and electron energy loss spectroscopy (EELS). The results are shown in fig. 6. It is clear that there is no metal diffusion or migration into either the oxide liner or the Si substrate. This confirms our electrical testing results and shows the oxide insulating layer and the diffusion barrier are working properly.
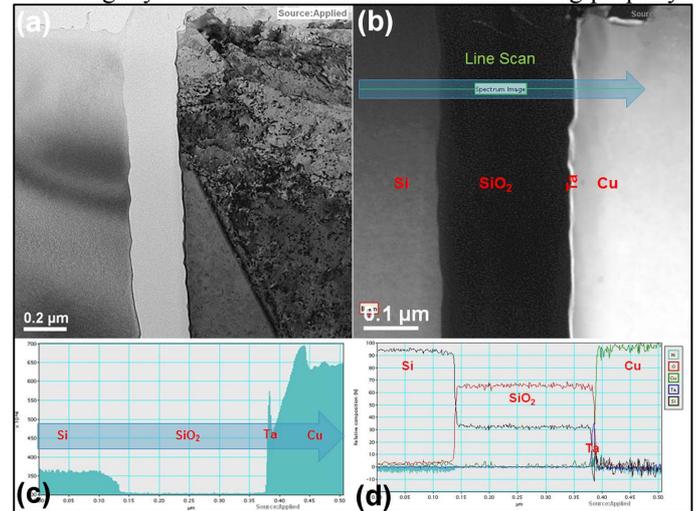

Fig. 6. (a) TEM image of SiO$_2$-Ta-Cu interface, (b) HAADF image of Si-oxide-Cu interface, (c) HAADF counts from STEM/EELS line scan, (d) relative composition of element Ta, Si, Cu, and O from EELS.

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