Endura® Ventura™ PVD
First Metallization Solution for High-Volume Manufacturing of Through-Silicon Vias

May 28, 2014
Semiconductor Pervasiveness

11% CAGR 2013-2018

Mobility continues to drive unit growth

Source: Gartner
Technology Landscape

High-End Device Demand
- Mobile Application Processors
- Microprocessors
- Enterprise Chips

Enhanced Performance
- Low Power Consumption
- High Bandwidth
- Form Factor
- Cost-Effectiveness

Packaging Innovation
- 3D Integrated Circuits
- Heterogeneous Integration
- 2.5D Packages
- Through-Silicon Vias

Applied’s precision materials engineering leadership enables high-performance integrated 3D chips
Vertical Integration for Higher Functionality

35% Smaller Package Size  
**FORM FACTOR**

50% Less Power Consumption  
**BATTERY LIFE**

8X Bandwidth Improvement  
**PERFORMANCE**

Wire Bonding  
2D

FI WLP  
2.5D

FO WLP  
TSV Interposers

Flip Chip  
TSV 3D ICs

Functionality/Performance/Form Factor

Heterogeneous Integration

Heterogeneous Stack
TSV Enables Revolutionary Architectures

Example: Hybrid Memory Cube

TSVs enable vertical stacking of DRAMs for higher bandwidth

Source: http://www.hybridmemorycube.org

Source: Applied Materials
Growing TSV aspect ratios require new PVD metallization solutions
Introducing Endura® Ventura™ PVD for TSV

- First PVD system designed for TSV metallization in HVM
- Innovation built on >20 years of Endura PVD leadership
- Integrated tantalum/titanium and copper chambers
- Cost-effective TSV barrier seed solution
Applied’s Complete Suite of TSV Products

**TSV Integration**
- Incoming Wafer
- TSV Etch
- CVD Liner

**Ventura PVD**
- PVD Barrier and Seed

**TSV Cu Plating**
- Excess Cu Polishing

The Asia Product Development Center integrates Applied’s TSV capabilities for customer R&D

**Ventura PVD system** extends **wafer-level packaging** leadership
TSV Features are Really Different!

TSV structures are 1000X deeper than copper vias

Deep TSVs are challenging for existing copper interconnect PVD
TSV Metallization – Gap Fill vs. Cost Dilemma

Cu Interconnect PVD in Cu Via

Cu Interconnect PVD in TSV

Ventura PVD in TSV

50nm:1X

50μm:1000X

Voiding due to weak coverage

Thicker films needed for void-free fill

TSV volume production possible only with robust gap fill at low cost
Robust Bottom and Sidewall Coverage

Cu Interconnect PVD in TSV

Ventura PVD technology improves coverage in TSVs by >50%

Voiding due to weak coverage

Thicker films needed for void-free fill

Ventura PVD technology improves coverage in TSVs by >50%
Continuous Barrier Coverage for Reliable TSVs

Interconnect Ta PVD
Discontinuous Coverage

Ventura Ta
Continuous Coverage

Barrier Thickness: 410nm

Source: IMEC
Barrier Thickness: 310nm

Side wall of TSV structure after HF exposure—barrier discontinuities highlighted by damage to underlying oxide liner

**Ventura PVD’s improved coverage** creates continuous copper barrier for reliable TSVs
Ventura PVD for Superior TSV Gap Fill

Superior coverage with thinner film promotes robust gap fill at lower cost
Flexible Configurations for HVM of TSVs

Industry-proven Ta barrier or lower-cost Ti barrier integrated with Ventura PVD copper seed
Costs of Ownership

Ti interconnect PVD (Ta/Cu)
Ventura Ta/Cu
Ventura Ti/Cu

Ventura PVD’s reliable and cost-effective Ti offers alternative to proven Ta barrier
Endura® Ventura™ PVD
First Metallization Solution for High-Volume Manufacturing of Through-Silicon Vias

- Integrated tantalum/titanium/copper PVD technology specifically for high aspect ratio TSVs
- Robust gap fill from superior coverage
- Lowers production cost with industry’s first titanium barrier option for TSVs
- >2X higher throughput than other copper interconnect PVD systems
- >30 chambers shipped in the past 18 months