Impact of Barrier Integrity on Liner Reliability in 3D Through Silicon Vias

Yunlong LI[1], Yann CIVALE[1], Yoshiyuki OBA[2], Andrew COCKBURN[3], Jin Hee PARK[4], Eric BEYNE[1], Ingrid DE WOLF[1,5], Kristof CROES[1]

[1]Imec, Kapeldreef 75, 3001 Leuven, Belgium
[2]Sony Corporation to IMEC, imec vzw, Kapeldreef 75, 3001 Leuven, Belgium
[3]Applied Materials Belgium, Kapeldreef 75, 3001 Leuven, Belgium
[4]Applied Materials, Santa Clara, CA
[5]KU Leuven, Dept. MTM, Kasteelpark Arenberg 44, 3001 Leuven, Belgium
e-mail: yunlong.li@imec.be

***Abstract*—For 3D chip stacking using Cu through silicon vias (TSV's), dielectric liner reliability is crucial and is closely related to the barrier integrity. In this study, two different Cu barriers are compared in terms of dielectric liner reliability. By using two stress modes, where different voltage polarities are applied to the TSV, the impact of barrier integrity on liner reliability is segregated and PVD Ti is shown to be superior to PVD Ta for our particular liner. The field acceleration factors are extracted using classical TDDB and from controlled ramp rates, where a good match is found between the two methods. When applying a positive voltage to the TSV during stress, a bimodal distribution of the TDDB lifetime is observed for the PVD Ta barrier. This is linked to a competition between Cu induced dielectric breakdown and intrinsic dielectric breakdown.**

Keywords-TSV; through silicon via; barrier/liner; barrier integrity; dielectric reliability; TDDB; controlled IV; dielectric breakdown; bimodal distribution; bi-mode stress

I. INTRODUCTION

3D chip stacking using Cu through silicon vias (TSV) is expected to be one of the key process technologies for extending Moore's Law for semiconductor industry [1]. During development, the TSV functionality has to be guaranteed by in-depth process optimization and characterization. For 3D stacking of advanced semiconductor chips, the TSV diameter is targeted at a few microns to reduce the wafer area consumption by the TSV as well the affinitive keep-out-zone (KOZ) [2][3]. On the other hand the TSV depth needs to be high enough in order to allow reliable wafer thinning and thin wafer handling. The large gap between these two dimensions results in TSV's with high aspect ratios and makes the TSV integration process and characterization a challenge. One critical aspect is to deposit a uniform and defect-free barrier layer on the TSV sidewall after dielectric liner deposition. Due to the high aspect ratio, the large vertical dimension and the 3D configuration, it is almost impossible to detect sub-nano scale defects (e.g. pinholes) in the integrated TSV barrier using standard physical characterization techniques. As a defective barrier degrades the insulating property of the oxide liner [4][5], electrical reliability characterization is needed to investigate the integrity of integrated TSV barriers. In our previous report [6], a fast reliability characterization method called "controlled IV (IV_{ctrl})" was proposed for a fast characterization of liner reliability and thus barrier integrity. In this study, both IV_{ctrl} and the traditional time-dependent-dielectric-breakdown (TDDB) tests are applied where two candidate barrier materials are compared in terms of dielectric liner reliability.

II. EXPERIMENTAL

The experimental samples are fabricated on 300 mm p-type wafers which have STI, PMD, contact, metal 1 (M1), metal 2 (M2) and passivation modules from imec's 65nm platform. The TSV integration uses a TSV middle scheme where the TSV module is inserted between the contact module and the M1 module [7][8]. The targeted TSV's have a 50 µm height and a 5 µm diameter, i.e. aspect ratio (AR) = 10. Within the TSV module, after Si dry etch, ~ 100 nm oxide liner is deposited on the Si sidewall by TEOS/O_3 pulsed CVD followed by PVD barrier/seed deposition. Afterwards, the deep trench via is filled with Cu by super-conformal electroplating [7][8][9]. Finally, the overburden Cu, the barrier and the liner on field are cleared by CMP [7][8]. At the end of the passivation module, 500 nm Al is deposited on the wafer backside for electrical contact.

The barriers investigated in this study are PVD Ta and PVD Ti. The Ta barrier metal is deposited in a standard PVD system and the Ti barrier metal is deposited in a novel PVD system which both increases the amount of sidewall coverage and has a barrier enhancing surface treatment. Additionally, it is expected that Ti will diffuse through the TSV Cu core during the following anneal steps to reinforce the as deposited Ti film and form a robust $TiSiO_3$ barrier encapsulating the entire TSV structure within the liner oxide.

Additionally, one wafer with the same TSV integration process and the same PVD Ta barrier but a lower TSV height (30 µm instead of 50 µm) is prepared to check the effect of TSV sidewall coverage. The TSV diameter is kept at 5 µm and thus AR is reduced to 6 and the TSV sidewall is believed to be fully covered by Ta barrier.

The test structure for reliability characterization is a TSV array with 15 TSV's connected in parallel to the Al bond pad

through M1 and M2, as shown in Fig. 1. The electrical stress is applied between the bond pad and the substrate.

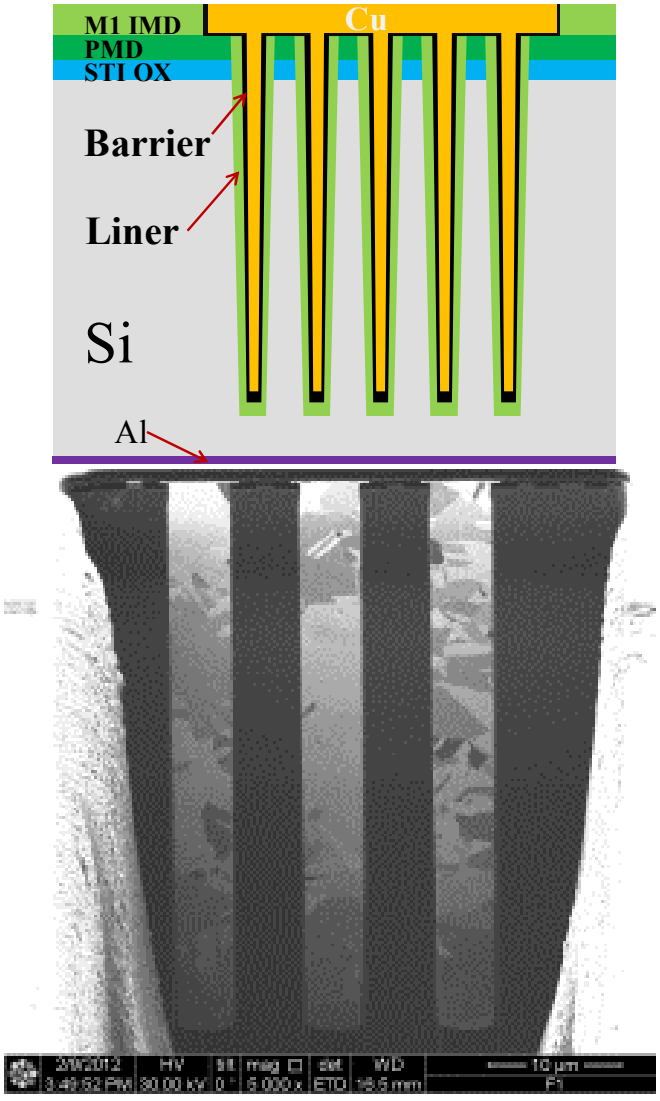

Figure 1 Schematic (top) and FIB (bottom) cross-sections of the test structure for TSV barrier/liner characterization.

Two reliability characterization methods are used: IV_{ctrl} [6] and TDDB. IV_{ctrl} is used for fast screening and TDDB is exploited for more in-depth understanding. For both methods, two stress modes are applied (Fig. 2): a Cu-confined mode (TSV connected to the low potential) and a Cu-driven mode (TSV connected to the high potential). For the Cu-confined mode, Cu drift towards the oxide liner is restricted by the reverse electric field and the effect of barrier defects is not included in the liner reliability result. On the other hand, during the Cu-driven mode stress, Cu can drift into the oxide liner through a defective barrier under the forward electric field and the contribution of barrier defects is included in the liner reliability data. By comparing the liner reliability data under these two stress modes, the impact of barrier integrity can be separated. Note that the concept of Cu-confined and Cu-driven stress modes has already been proven in [10].

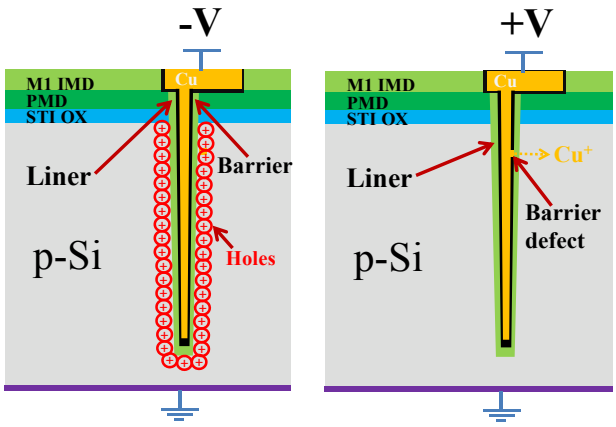

Figure 2 Two stress modes to segregate the effect of barrier integrity on liner reliability: Cu-confined (left) and Cu-driven (right).

III. Results and Discussion

A. Controlled IV (IV_{ctrl})

The IV_{ctrl} results for the two barrier metals under the two stress modes are summarized in Table 1, where the TDDB field acceleration factor γ of the E-model ($t_{50\%} \sim \exp(-\gamma \cdot E)$) is calculated from the slope of the breakdown voltage vs. the voltage ramp rate [6]. Since TDDB lifetimes are strongly field dependent, a high γ means long lifetime when extrapolated to use condition. Based on our experimental data and literature [4][11], an empirical criterion is set: a $\gamma > 8$ decade/(MV/cm) suggests good reliability, while $\gamma < 4.5$ decade/(MV/cm) indicates bad reliability for SiO_2 liners. For TSV's with a PVD Ti barrier, the extracted γ is above 8 decade/(MV/cm) for both Cu-confined mode and Cu-driven mode. This means that the liner reliability is high enough when the electrical confinement of Cu drift is released and this PVD Ti layer is an effective Cu barrier. For the TSV's with the PVD Ta barrier [Table 1], the γ value under the Cu-driven mode is much lower than 8 decade/(MV/cm) while the one at Cu-confined mode is much higher, indicating that Cu drift into oxide liner occurs under the forward electric field and significantly degrades the liner reliability. Therefore, this PVD Ta barrier is defective based on the IV_{ctrl} test. Note that in this and the following session, the calculated γ for a good barrier/liner system varies substantially from device to device and especially between different stress modes. We believe that this is due to the fact that γ estimates are highly dependent on liner thickness. As liner thicknesses are not well-controlled in TSV's [7][8], higher differences in γ are expected. Besides, stressing with different polarities leads to different mechanisms of electron injection into the liner, which can also result in the above mentioned differences in γ.

For IV_{ctrl}, one thing to consider is the substrate carrier distribution. The two stress modes (Cu-confined and Cu-driven) of IV_{ctrl} have different carrier distributions in the Si substrate, where for p-Si, the Si is in accumulation in the Cu-confined mode and in depletion in the Cu-driven mode. This may induce concerns when directly comparing the reliability data of these two modes. The influence of carrier distribution can be checked by measuring two TSV samples with the same integration scheme but opposite substrate types. In our investigation, TSV with PVD Ta barrier integrated in a 300

mm n-type wafer is also measured with IV_{ctrl} in both Cu-confined and Cu-driven modes and the extracted γ values [Table 1] are in good match with the corresponding stress mode from the p-type substrate sample. This demonstrates that the influence of carrier distribution is negligible and the reliability data in these two stress modes are directly comparable.

B. Time dependent dielectric breakdown (TDDB)

TDDB measurements have been collected to gain more in-depth understanding. Note that measuring TDDB lifetimes on TSV-systems take much longer time because the high variation in effective liner thicknesses leads to high σ's of the lognormal distribution of failure times. The lognormal distributions of TDDB lifetime data under the two stress modes are given respectively, in Fig. 3 for PVD Ti and in Fig. 4 for PVD Ta. Using maximum likelihood estimation (MLE) of the TDDB data, the lifetime parameters including the field acceleration factor γ are extracted and summarized in Table 2 and Table 3.

For TSV with PVD Ti barrier [Fig. 3, Table 2]: TDDB tests under the two stress modes show similar γ values as those from IV_{ctrl} measurements. This confirms that PVD Ti is an effective barrier for reliable 5×50 μm TSV integration. As mentioned before, the wide spread in TDDB lifetimes is attributed to the high liner roughness on the TSV sidewall.

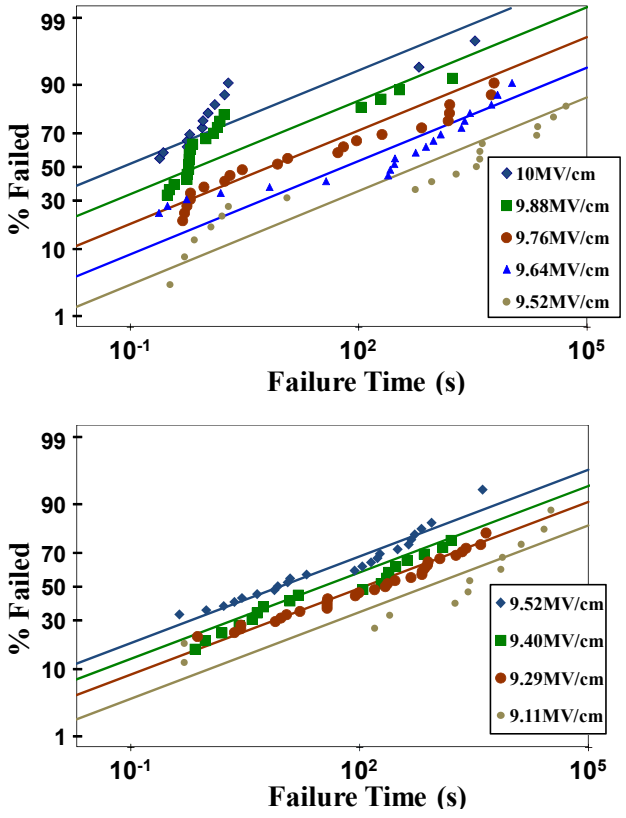

Figure 3 Lognormal fitting of TDDB data for TSV's with PVD Ti barrier stressed at two modes (Cu-confined mode at the top and Cu-driven mode at the bottom).

Table 1 Summary of TDDB field acceleration factors extracted from IV_{ctrl} measurement (first three samples have a AR=10) [unit: decade/(MV/cm)].

	Cu-confined	Cu-driven
PVD Ta	8.9	3.6
PVD Ti	24.4	8.6
PVD Ta (n-Si)	8.5	2.4
PVD Ta (AR=6)	9.8	4.1

Table 2 Summary of fitted reliability parameters (with 95% confidence bounds) from TDDB measurements for TSV with TEOS/O_3 liner and PVD Ti barrier.

	γ [decade/ (MV/cm)]	σ
Cu-confined	22.1 -/+ 0.2	4.5 -0.8/+1.2
Cu-driven	11.1 -/+ 0.1	6.5 -0.7/+0.9

For TSV with PVD Ta barrier [Fig. 4, Table 3]: The Cu-confined stress mode shows very similar TDDB lifetime distributions compared to that of PVD Ti and gives a γ value of ~12.5 decade/(MV/cm) which is similar as the one extracted from the IV_{ctrl} test. The higher field stresses in the Cu-driven mode show a strong bimodal distribution in failure times, further referred to as 'main' and 'tail' in the graph. For lower field (≤7 MV/cm) stresses, this bi-modal trend is not present. By doing bimodal fitting analysis, the reliability parameters can be obtained for each mode (Table 3), where totally different γ values are obtained and lead to significantly different lifetimes at use condition. γ for the tail part is much higher than the main part and is comparable to that of the Cu-confined mode. γ for the main part is close to that from IV_{ctrl} test at the same stress mode. The main part of the distribution is hypothesized to be defective barrier induced dielectric failure, while the tail part is attributed to non-barrier related intrinsic dielectric failure. Thus the bimodal distribution at Cu-driven mode can be explained by the competition of two failure mechanisms: Cu induced dielectric failure and intrinsic dielectric failure. Here, it looks contradictory that the more intrinsic dielectric breakdown is happening faster than the Cu induced dielectric breakdown. However, considering the high aspect ratio of Cu TSV and the rough sidewall surface after Si dry etch [7][8], this contradiction can be explained by two competing failure mechanisms dominant at non-overlapping positions. For Cu induced dielectric breakdown, it happens in the liner next to the barrier defect whereas for the intrinsic dielectric breakdown, the failure position is at places with enhanced electric fields due to the rough sidewall, e.g. the scallops near the TSV bottle neck. These two kinds of positions are not always overlapping. Thus, when stressed at very high fields, the enhanced electric field at the rough liner surface gets close to the dielectric breakdown field and triggers breakdown first. When the stress field is lower, the enhanced field is still well below the dielectric breakdown field and Cu has enough time to drift through a defective barrier and trigger dielectric failure first. Therefore, for use conditions which are much lower than the TDDB stress conditions, only Cu induced dielectric breakdown is expected

to happen for this PVD Ta barrier. In Fig. 5, a lifetime plot ($t_{50\%}$ vs. E) shows that we do not meet the required 10 years spec with this PVD Ta barrier while it is met for the case with the PVD Ti barrier.

One possible reason for the poor TSV liner reliability at Cu-driven mode is incomplete TSV sidewall coverage by the Ta barrier due to the high AR. However, for TSV's with the same integration process but a much lower aspect ratio (AR=6) are tested with IV_{ctrl} where full sidewall coverage is expected, similar γ values are collected as those of the AR=10 TSV's (Table 1). This excludes the possibility of incomplete sidewall coverage induced liner degradation. As already known in literature [12][13], TEOS based oxide can absorb moisture from the ambient. These moisture components can be the oxygen source for Ta barrier degradation. Here we believe that this is the reason for the failing PVD Ta barrier. Further understanding is needed where different liners need to be evaluated in the future.

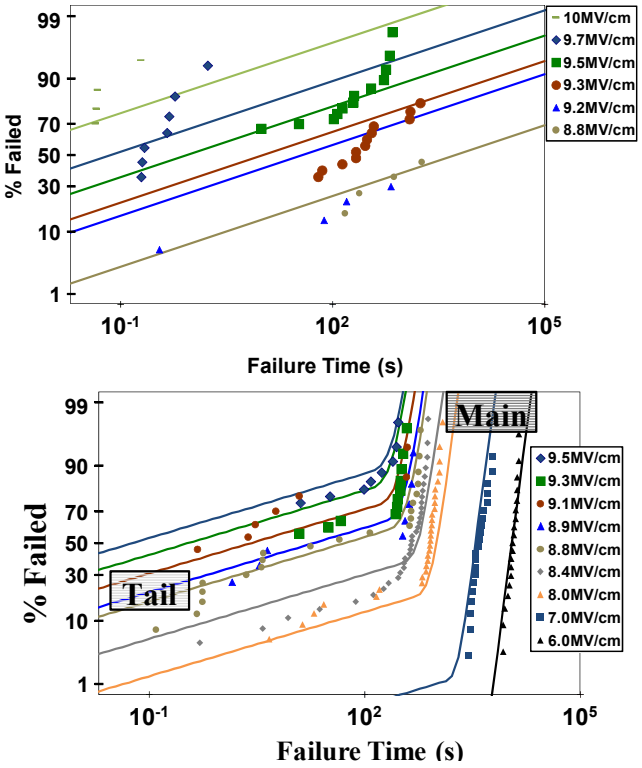

Figure 4 Lognormal fitting of TDDB data for TSV's with PVD Ta barrier stressed at Cu-confined mode (top) and Cu-driven mode (bottom).

Table 3 Summary of fitted reliability parameters (with 95% confidence bounds) from TDDB measurements for TSV with $TEOS/O_3$ liner and PVD Ta barrier.

	γ [decade/(MV/cm)]	σ
Cu-confined	12.5 -0.3/+0.1	5.84 -0.77/+1.05
Main of Cu-driven	0.77 -/+ 0.01	0.16 -0.03/+0.04
Tail of Cu-driven	9.8 -/+ 0.1	6.37 -0.80/+1.11

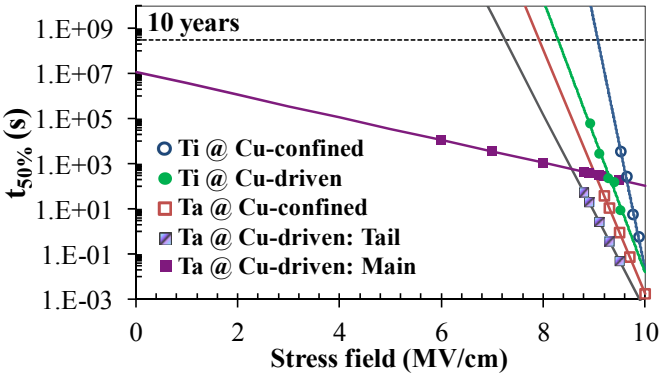

Figure 5 E-model based lifetime plot of TSV's with $TEOS/O_3$ liner for PVD Ti and PVD Ta barriers at two stress modes.

IV. Conclusion

For 3D Cu TSV's, it is shown in both controlled IV and TDDB tests that barrier integrity has significant impact on dielectric liner reliability. For high aspect ratio (e.g. 5×50 µm) TSV, although the liner is quite thick and conformal over the whole TSV sidewall, a defective barrier may still happen and result in extremely short use lifetimes. It is also shown that PVD Ti barrier is superior to PVD Ta in terms of reliability for high aspect ratio TSV integration, where the failing Ta-barrier is linked to an interaction between the Ta and the highly moisturized liner used in this study.

For the defective Ta barrier, bimodal TDDB lifetime distributions are observed and explained by the competition of two failure mechanisms during electrical stress which means stressing the TSV barrier/liner system at lower fields is essential for a correct understanding and evaluation of the TSV barrier integrity and liner reliability.

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