Millisecond anneals becoming a growing portion of SAM

Source: Gartner Dataquest, September 2009
Building a Transistor

Gate Dielectric → Gate Stack Etch → Implant & USJ Anneal → Spacer

Recessed Source/Drain → Selective Epi → Nickel Deposition → Ni Diffusion Anneal

Phase Transformation to NiSi Anneal → Stress-Inducing Nitride → HARP for Pre-Metal Dielectric → Transistor On Increased Drive Current

Anneal steps are key to device scaling
Evolution of Single-Wafer Anneals

Benchmark performance, consistently delivered by Applied Materials
Annealing Technology Drivers

- **Transistor Scaling**
  - Minimized diffusion for shallower junctions
  - High dopant activation
  - Thinning nickel silicide contact layers
  - Avoiding yield-inhibiting piping defects

**Future Applications**

- **High-k/Metal Gate**
  - Work function optimization

- **Memory Yield Enhancements**
  - Minimizing defects in cell array
  - Applying logic junction engineering advances to periphery

- **3D Devices**

**Improved silicide contact is key to scaling without degrading leakage**
Building a Transistor

- Gate Dielectric
- Gate Stack Etch
- Implant & USJ Anneal
- Spacer
- Recessed Source/Drain
- Selective Epi
- Nickel Deposition
- Ni Diffusion Anneal
- Phase Transformation to NiSi Anneal
- Stress-Inducing Nitride
- HARP for Pre-Metal Dielectric
- Transistor On Increased Drive Current

Advanced anneals are key to scaling
**Trend toward Millisecond Anneal**

<table>
<thead>
<tr>
<th>Main Anneal Steps in FEOL Flow</th>
<th>Logic (65nm) Poly Gate</th>
<th>Logic (45nm) Poly Gate</th>
<th>Logic (32nm) Hi-k Metal Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre Gate Anneals</td>
<td>Soak</td>
<td>Soak</td>
<td>Soak</td>
</tr>
<tr>
<td>Source-Drain-Poly Implant Activation and Diffusion</td>
<td>Spike</td>
<td>Spike</td>
<td>Spike</td>
</tr>
<tr>
<td>Activation Boost</td>
<td>Millisecond</td>
<td>Millisecond</td>
<td>Millisecond</td>
</tr>
<tr>
<td>HKMG Work-Function Optimization Anneal</td>
<td>Millisecond</td>
<td>Millisecond</td>
<td>Millisecond</td>
</tr>
<tr>
<td>Ni Silicidation Diffusion</td>
<td>Soak</td>
<td>Soak</td>
<td>Soak or Millisecond</td>
</tr>
<tr>
<td>NiSi Phase Transformation</td>
<td>Soak</td>
<td>Soak or Millisecond</td>
<td>Millisecond</td>
</tr>
</tbody>
</table>

Similar use of millisecond can be made in DRAM periphery

**Need higher activation temperature, improved leakage control, shorter dwell time**
Trend toward Millisecond Anneal

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**Spike to Millisecond**
Lower spike temperatures reduce activation in ultra-shallow junctions; need diffusion-less boost

**Millisecond Delivers:**
- Thinner effective gate oxide at temperatures >1150°C
- Added source-drain activation without added diffusion
- Minimal impact on limited thermal budget

**Soak to Millisecond**
Thinner silicides without compromising conductivity or yield

**Millisecond Delivers:**
- Improved dopant activation at higher temperature
- Super-fast ramp up/down without deactivation typical of long exposures at mid-range temps
- Fewer leakage-inducing defects through steep temperature profile

Nickel silicidation is the most challenging millisecond anneal
The Ideal Time-Temperature Profile for NiSi

Key parameters to consider

**Preheat**: Must be low enough to avoid uncontrolled diffusion

**Jump temp**: Must be high enough to enable optimal activation w/o wafer breakage or agglomeration

**Dwell time**: Must be short to avoid wafer bow and breakage

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,000</td>
<td></td>
</tr>
<tr>
<td>900</td>
<td></td>
</tr>
<tr>
<td>800</td>
<td></td>
</tr>
<tr>
<td>700</td>
<td></td>
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<tr>
<td>600</td>
<td></td>
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<tr>
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</tr>
<tr>
<td>300</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

Above profile is key to enabling optimal nickel silicide
NiSi Morphology Improvement

Lowest interface roughness achieved with reduced RTP-1 soak temperature and millisecond RTP-2

NiSi Piping Defects Reduction

TEM Top View

Piping Defects Count

Normalized Defects (%)

<table>
<thead>
<tr>
<th>RTP-1 anneal:</th>
<th>T1 Soak</th>
<th>T1-40°C Soak</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTP-2 anneal:</td>
<td>T2 Soak</td>
<td>T2+400°C Millisecond</td>
</tr>
</tbody>
</table>

Based on e-beam Bright Voltage Contrast (BVC) count on a pattern wafer post WCMP


Lowest piping defects count achieved with combination of reduced RTP-1 soak temperature and millisecond RTP-2
Several percent drive current gain achieved by enhancing nickel silicide contact using millisecond annealing with low temperature RTP-1 soak.
The Ideal Time-Temperature Profile for NiSi

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<tr>
<th>Temperature</th>
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<tbody>
<tr>
<td>250°C or less</td>
<td>0.25msec</td>
</tr>
<tr>
<td>350°C</td>
<td>0.4msec</td>
</tr>
<tr>
<td>400°C</td>
<td>0.8msec</td>
</tr>
<tr>
<td>500°C</td>
<td>200°C</td>
</tr>
<tr>
<td>600°C</td>
<td>300°C</td>
</tr>
<tr>
<td>700°C</td>
<td>400°C</td>
</tr>
<tr>
<td>800°C</td>
<td>500°C</td>
</tr>
<tr>
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<td>600°C</td>
</tr>
<tr>
<td>1,000°C</td>
<td>700°C</td>
</tr>
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**Graph**

Delivered by Applied Materials’ Vantage Astra system
Applied Vantage® Astra™ DSA System

- **Uniquely powerful silicidation**
  - Up to 5% greater device speed
  - Higher yields enabled by up to 15x lower leakage
  - Less wafer stress

- **Versatile dynamic millisecond anneal**
  - Broad range of processing conditions
  - Ambient control
  - Extendible to high-k/metal gate applications

- **Compact, reliable, cost-effective**
  - Simple, compact and smart chamber design
  - Solid-state laser with prolonged lifetime
  - > 40 WPH per two-chamber system
  - Compatible with an RTP chamber on same system as hybrid

**FAST. SMART. RELIABLE.**
Simply Better Anneal
Applied Vantage Astra DSA System

FAST. SMART. RELIABLE.
Scan and Overlap Concept

Beam Profile View

Laser Beam Spot

Scan 1
Scan 2

Scan 1 Scan 2
Dynamic Surface Annealing (DSA)

Three dimensional steady state result for 810nm

Modifying scan speed determines anneal dwell (exposure) time

Simulation results on bare silicon

Scan direction
Availability

FAST. SMART. RELIABLE.

weekly monitoring over 1 year
Productivity: Competitor Comparisons

WAFERS PROCESSED

- Applied Vantage Astra
- Flash Competitor
- Laser Competitor

TIME

FAST. SMART. RELIABLE.
Applied Vantage Astra DSA System

- **FAST**
  - Higher throughput
  - Shorter dwell time

- **SMART**
  - Compact design
  - Broad process window
  - Ambient control

- **RELIABLE**
  - Solid-state laser
  - Reduced wafer stress
  - Based on the production proven Vantage

Simply Better Anneal