NANOCHIP Technology Journal

EXTENDING TRANSISTOR TECHNOLOGIES IN THE 3D ERA

IN THIS ISSUE
- Fin Doping With Hot Implant
- Plasma Doping of High Aspect Ratio Structures
- Integrating Millisecond and Spike Anneals

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TO OUR READERS

This issue of Nanochip focuses on advances and innovations taking place in front-end-of-line processes as the transition to 3D device architecture gathers momentum and planar scaling pushes its boundaries. A primary catalyst of change is the FinFET, whose design poses diverse challenges for gap fill, CMP, implant, metal deposition, capacitance control, contact resistance, and channel mobility enhancement. Our feature article reviews these and solutions already in place or under development.

We also review two advances in ion implantation. One approach employs hot implantation to solve the issue of crystallinity damage in narrow fins that exacerbates junction leakage and parasitic resistance. A higher substrate temperature during implantation enhances defect annihilation during the subsequent anneal, thereby raising the dose threshold for the onset of amorphization. In other applications, plasma doping is addressing challenges posed by high aspect ratio (HAR) features in advanced memory and CMOS image sensor devices. The inherent conformality and tunability of plasma doping are major advantages over other approaches in applications such as HAR staircase contacts. This technology also solves the issue of reducing dark current for CMOS image sensor manufacturers as the lower energy levels used in plasma doping avoid the end-of-range damage responsible for this undesirable effect.

While emerging 3D solutions are claiming much of the industry’s attention, innovations continue to enhance the performance of planar devices. We demonstrate that integrating laser millisecond anneal and spike anneal achieves optimum dopant activation while preserving ultra-shallow junction profile and depth. The low stabilization temperature of laser millisecond anneal precludes formation of dopant-deactivating interstitials. The spike anneal can thus achieve maximum effect, which in turn enhances transistor drive current.

These studies are representative of our commitment to pushing the frontiers of our knowledge in pursuit of cost-effective solutions to our customers’ high-value problems. We trust you will find them of interest and value.

Cover: The FinFET structure avoids short-channel effects that are limiting planar device scalability and eases the power vs. performance tradeoff. While leading the industry into the 3D era, the FinFET is helping to shift the design paradigm from packing density to best performance per watt.
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Extending Transistor Technologies in the 3D Era

KEYWORDS
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Contact
FinFET
High-k Metal Gate
Implant
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Spacer

The modern MOSFET era has undergone numerous changes in transistor materials and fabrication, a trend expected to accelerate from the 2x nm node onward to satisfy growing demands for mobility and connectivity. Power economy, and greater speed and packing density are the predominant factors driving today’s transistor scaling and design innovations. This companion article to the Volume 11, Issue 1, 2013 overview of interconnect advances examines specific challenges faced by transistor technologies and solutions for their continued scaling.

Since the introduction of planar IC process technology, feature size and density have scaled at a rate of approximately 30% linear reduction per generation. This scaling has provided many benefits, including continuous cost reduction, performance improvement, and power reduction for IC technology and related products. At each generation, the industry has surmounted technology challenges to enable the scaling.

Over the last several nodes, in addition to scaling, significant changes have been made in materials and architecture used to fabricate transistors. The 90nm node saw epitaxial SiGe source drain (S/D) stressors;[1] the 45nm node saw adoption of high-k metal gate (HKMG);[2] while 22nm introduced the non-planar FinFET[3] and ushered in the era of 3D transistors for logic. These tri-gate or FinFET transistors improve electrostatic control of the channel region, reducing off-state leakage, and enabling continued gate length scaling and greater transistor density.

The CMOS industry has made great progress in gate length (Lg) scaling, averaging 28% per generation from the micron scale to 65nm.[1245] In practice, Lg has scaled at a slightly slower rate than the overall device pitch reduction of 30%; as a result, the contact and spacer width have scaled at a slightly faster rate. However, Lg scaling stalled at the 45nm and 32nm nodes, primarily because of difficulty maintaining threshold voltage (Vth) control at short Lg. At shorter Lg, the gate and drain compete for control of the channel, leading to a Vth degradation known as drain-induced barrier loading (DIBL) at higher drain bias (Equation 1).[6] DIBL is improved if gate oxide capacitance increases or junction depth decreases. It degrades from lower Lg and reduced \( \varepsilon_{sc} \) (dielectric constant of the semiconductor). Despite the introduction of HKMG, progress in DIBL improvement stalled after 45nm due to physical challenges in doping and gate oxide thickness reduction.

\[
\text{DIBL} = 0.80 \frac{\varepsilon_{sc}}{\varepsilon_{ox}} EI \times V_{ds} \quad [1]
\]

\[
EI = \left(1 + \frac{X_f}{T_{ox-el}} \right)^{-1} \frac{T_{ox-el}}{L_{el}} \frac{T_{dep}}{L_{el}}
\]

DIBL can be improved, however, by using a multi-gate device, which increases gate coupling to the channel and effectively makes the junction depth shallower. In the planar device, a capacitor lies between the gate and the channel and between the drain and the channel (Figure 1a). These two capacitors compete to control the channel potential. As the gate must remain in control, the ratio of gate and drain capacitance must be controlled. FinFET topography adds multiple gates on the side of one channel (Figure 1a), improving the gate coupling ratio. This can be thought of as effectively reducing the junction depth to half the fin width \( W_{fin} \). Thus, the FinFET can be scaled by reducing the \( W_{fin} \) for each generation as Lg is also reduced.[7] Although the FinFET is a practical way to fabricate double gate devices on a silicon wafer, it introduces many new challenges, including pitch scaling and conformality, and complex topological requirements (Figure 1b).
Table 1 shows the new challenges to be addressed in each of the key process flow modules, with potential solutions for both early-generation and highly scaled FinFET technologies. In the following sections, we review those challenges and their solutions.

### Fin and Dummy Gate Formation

The width of a FinFET is determined by the perimeter of the fin, thus fin pitch should be no larger than the fin perimeter to maintain current density. A small fin pitch allows for a shorter fin to be used, simplifying later etch and fill steps. At a specific node, FinFET STI pitch can be 30% shorter than planar, given the challenge of forming a tall structure. In addition, to achieve the tall and narrow fin needed to control DIBL, a rectangular shape is preferred. This leads to a vertical profile at the STI gapfill step, making void-free fill extremely challenging. Using a flowable gapfill process with a low glass-transition temperature solves this issue.

Device perimeter is controlled by the fin STI recess. This mandates a precise, uniform etch to control recess depth. It is also critical to avoid modifying the fin profile during the recess; a process with very high selectivity (> 100:1) should be used to remove the oxide without changing $W_{fin}$.

The FinFET requires precise control of the gate structure, which undergoes many process steps, including spacer etch, gate etch, replacement gate, and self-aligned contact (SAC) formation. The latter three steps involve CMP. It is noteworthy that gate lithography requires a planarization step for critical depth-of-focus control. CVD poly deposition over fins results in a non-planar structure (Figure 2a), necessitating a polish step to produce a flat surface and precise gate layer thickness. Spectroscopy-based in-situ endpoint control enables the requisite nanometer-scale height consistency to be achieved (Figure 2b).

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**Table 1.** Challenges and solutions in major CMOS device fabrication steps for FinFETs.

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**Figure 1.** (a) Comparison of gate coupling in planar and fin devices. Gate coupling from multiple directions in the fin device helps the gate to control the channel potential and the device to switch on and off. (b) Structure-related challenges in fabricating a FinFET.
Junction

Fin sidewalls must be doped to form the source/drain extension (SDE) junction. This requires a very low-damage (ribbon beam), high-tilt implant technique with advanced angle control. When SDE implants are made at the 1e15 dose range required for good external resistance, the Si structure is amorphized. In a planar structure, the S/D dopant activation anneal re-crystallizes the material. In a FinFET, however, the greater distance from the fin to the crystalline base allows multiple crystals to nucleate, producing a polycrystalline structure. A low-damage heated implant solves this issue. It avoids the amorphization while delivering the needed dose, thereby creating a highly doped, crystalline, post-anneal structure.

Angled implants have been used for many generations of CMOS devices. As design rules have scaled, implant masking has become more difficult because the thick photoresist (PR) required results in shadowing (Figure 3). However, shadowing can be substantially reduced by using a thin conformal hard mask formed from a material, such as carbon, that can be easily removed with high selectivity and no damage to the fins. Conformal CVD carbon hard mask thus enables continued design rule scaling with angled implants.

HKMG

In recent planar MOSFETs, replacement high-κ metal gate (RMG) technology has been used to maintain good work function and gate leakage on a device with very thin electrical oxide thickness (approximately 1nm). Adopting the RMG approach for FinFETs requires conformal, uniform deposition of all the thin metal gate film layers on the sides and top of the fin (Figure 4a). Furthermore, Lg scaling requires that the entire multi-layer structure fit into a gate feature less than 20nm wide. Typically the cap and etch stop films are approximately 2nm thick with a work function metal approximately 3-4nm thick.
After the work function and cap layers are deposited, the remaining space is filled with a highly conductive material (e.g., Al or W), which helps the gate electrode deliver the fast switching time needed for picosecond-level gate delays. In the Figure 4a example, approximately 6nm remains for the metal fill. Figure 4b shows that the conductance vs. trench width curve of traditional CVD W fill preceded by a TiN barrier and diborane-W nucleation does not scale well below 10nm. The trench is filled with resistive TiN and nucleation layers, leaving no room for the conductive fill. Ultra-thin ALD metals with band-edge work function and low resistivity resolve this issue below 10nm and deliver better conductance than W fill.

**Capacitance Control**

FinFETs heighten the challenge of controlling parasitic capacitances. A particularly undesired class of parasitic is the Miller Capacitance (Cov) between the gate and drain. When the transistor turns on, the direction of gate potential is the opposite of the drain, so the Cov sees a voltage change of 2 Vcc, rather than just 1 Vcc. Contact-to-gate capacitance (Ccg) is an important component of Cov. The FinFET gate is approximately two to three times taller than that of a planar device, thus increasing the surface area of the capacitor formed with the spacer dielectric between the gate and the contact and S/D epi structure.

One necessary capacitor is the gate capacitor (Cgate), which turns on the channel. With each node, the Cgate scales by the relationship Cgate=Cox*Lg. Lg decreases by approximately 28%, which drives down Cgate, reducing power. Although Cgate is shrinking, so is spacer width; hence Ccg is increasing. Consequently, the ratio of Ccg to Cgate is growing rapidly (Figure 5). Some approaches to managing this are to minimize the contact width, reduce the dielectric constant (k) of the spacer material, and control the width of the S/D epi region.

**Contact and Spacer**

Contact width must be scaled because it is part of the gate pitch. With each generation, contact width decreases while drive current remains constant or increases. Contact resistance per unit area must therefore improve by approximately 30% per generation, consistent with Lg scaling.

The largest component in contact resistance is the interface resistance, which is limited by tunneling through a Schottky barrier at the metal/semiconductor interface. The two primary means by which to improve that barrier are higher surface doping and barrier height reduction. Si doping of approximately 2-3e20 atoms/cm³ has been achieved with boron and phosphorous (P) implant and annealing. It is important...
to maintain that doping concentration through the silicide process during which diffusion or deactivation can reduce the active doping level. In seeking a means of addressing this concern, studies have shown that implanting P and selenium after silicide formation, with a laser anneal for activation, can substantially improve the interface resistance.\(^\text{[10]}\)

**FinFET Mobility Enhancement**

Mobility enhancement is one of the effective techniques for improving logic device performance. Starting at the 90nm generation, channel strain has been used to significantly improve mobility, resulting in higher transistor drive current.\(^\text{[1]}\) The extension of channel strain has been significantly refined with embedded S/D stressors on planar devices, more than doubling drive current in PMOS devices.\(^\text{[2]}\) Stressors have also been implemented in FinFET technology,\(^\text{[3]}\) with the observation that an unmerged S/D stressor provides the best strain transfer. However strain transfer is less efficient than in planar devices due to the 3D FinFET structure.\(^\text{[11]}\)

Beyond stressors, further mobility enhancement can be achieved using a channel material with higher mobility than silicon. Germanium (Ge) has high hole mobility and indium gallium arsenide (InGaAs) has high electron mobility compared to Si. High-mobility fin channels can be formed by the STI replacement technique illustrated in Figure 6. First, STI is formed using a traditional process. Either thick STI nitride is used or a tall Si pillar is formed. After STI CMP, the STI nitride or Si is etched, and a narrow trench is formed. A selective epitaxial process can then be used to fill the trench with the desired high-mobility channel material. This approach has produced high-quality epitaxial fins. Following epitaxy, the fins are planarized to remove facets and overburden, and STI recess is then performed.

**CONCLUSION**

The introduction of the FinFET device architecture to facilitate continued downward scaling of device size brings a new set of manufacturing and materials challenges. Increased fidelity to form the smaller devices is provided by intrinsically precise technology, such as ALD, and enhanced control techniques, such as in-situ endpoint monitoring in CMP. High aspect ratio structures and conformality requirements shift manufacturing methods to compatible techniques such as flowable CVD for high aspect ratio gapfill, heated implants for doping thin structures, and ALD metal gate for metal deposition on vertical structures. Epi-grown semiconductors facilitate continued improvement in device mobility and performance. As CMOS technology continues to scale, sustained innovation in hardware technology and materials engineering makes possible ongoing development of next-generation devices.

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**Figure 6.** Formation of Ge fins using epi in a replacement trench structure.
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Fin sidewall doping and activation, crystallinity control of the fin, junction profile, and leakage control on the fin are new challenges faced in FinFET fabrication. Narrower fins are more prone to crystallinity damage by ion implant, leading to greater junction leakage and fin parasitic resistance. Hot arsenic (As) implant has demonstrated damage-free fin source/drain extension (SDE) and halo doping, producing fivefold improvement in fin line conductance and more than tenfold reduction in junction leakage over room-temperature (RT) implant.

FinFET technology was introduced at the 22nm technology node to suppress device short channel effects (SCE);\(^1\) the fin and the gate CD will continue to scale with future technology nodes. Narrow fins improve device SCE control. For optimal device drive current, the sheet resistance of the SDE must be minimized. Ion implantation is the leading candidate for junction formation with the advantages of precision dose and energy control, which enable precision tuning of transistor performance and reduced device variability.

The traditional low-energy, high-dose As ion implant for nSDE can fully amorphize the narrow fin, and results in damaged fin crystallinity upon activation anneal\(^{12,21}\) and leads to high parasitic resistance and junction leakage. The amorphization results from a critical balance between damage generation and its annihilation.\(^{14}\) Raising the substrate temperature during ion implantation, referred to as hot implant, enhances defect annihilation or dynamic anneal, which increases the dose threshold for the onset of amorphization.

This article presents work done using hot implant to achieve damage-free As fin SDE doping and halo doping. Below a fin width \(W_{\text{fin}}\) threshold of 15nm at which the RT As-implanted fin became polycrystalline, hot implant resulted in a fivefold improvement in fin line conductance and tenfold improvement in junction leakage.

**EXPERIMENTAL STUDIES**

The fin resistor structures were fabricated in the Maydan Technology Center at Applied Materials. P-epi-on-P+ Si substrates in the \(<100>\) orientation were used with fin structures patterned in the \(<110>\) direction. Figure 1a details the fin fabrication process. Thin layers of oxide and SiN were thermally grown on a Si substrate, followed by deposition of an advanced patterning hard mask and SiN mask-open layers. Litho and etch were conducted and trimming was used in the etch process to obtain the desired \(W_{\text{fin}}\). After a post-etch clean, a liner was grown by rapid thermal oxidation and followed by sub-atmospheric CVD oxide deposition for shallow trench isolation (STI) gap fill. Oxide CMP preceded pad nitride removal in hot phosphoric acid. Oxide recess was carried out using dry oxide etch to expose the fin. Final fin height was 40nm, with a minimum width of 6nm.

Figure 1b illustrates the fin resistor layout with probe pad assignments. A four-terminal resistance measurement was used for accuracy. In the layout, 150 fins were tied together in parallel to obtain good average fin resistance per fin. The fin resistor was formed by implanting n-type dopant As into the top portion of the fin at low-energy and high dose to mimic nSDE implant. Isolation from the substrate was achieved by the n+p junction formation in the fin. The fin line resistance was measured by forcing current through the pads \(I^+\) and \(I^-\), and sensing the voltage drop between probe pads \(V^+\) and \(V^-\). The diode reverse-bias junction leakage was measured by using a probe pad \((I^+)\) as one electrode and the substrate as the other electrode.
Beam line implant was carried out using a high current implanter for As SDE implant and a medium current implanter for As halo implant. Both systems maintained the wafers at elevated temperatures during the ion implant. A spike anneal was used for post-implant dopant activation.

RESULTS

Two hot As implant scenarios were compared with results from RT implant: low-energy/high-dose implantation and low-dose/high-energy implantation.

Low-Energy, High-Dose Implant
SDE implants were performed on fins in dual mode (from both sides) with 1E15 cm\(^{-2}\) dose, 3keV ion energy, 45° tilt angle, and 90° twist angle relative to the fin orientation. Different substrate temperatures were used. A 1020°C spike anneal followed to activate the dopant. Reverse-bias junction leakage current was measured on the 15nm wide fin diodes at 5V, and the cumulative distribution of leakage current was plotted for both hot and RT implant (Figure 2a). The fins that received hot implant showed more than tenfold reduction in leakage current compared with a RT implant. These results suggest that fins receiving a hot implant have much better post-spike-anneal crystallinity.

Fin resistance was measured following spike anneal and the fin conductance was plotted as a function of \(W_{\text{fin}}\) for both hot and RT As SDE implants (Figure 2b). Fins that received a RT implant showed an abrupt increase in fin conductance for \(W_{\text{fin}}\) between 15nm and 20nm, and a progressive increase for widths exceeding 20nm. Fins implanted at the higher temperature showed a steady progressive increase in fin conductance as \(W_{\text{fin}}\) increased. Overall, fins receiving hot implant were more conductive, with a fivefold improvement observed in fins less than 15nm wide.
To investigate the abrupt change in fin conductance in narrow fins for RT implants, fin crystallinity was analyzed by cross-sectional transmission electron microscopy (XTEM). The crystalline Si (c-Si) is the dark region in the XTEM, while the amorphous Si is the homogeneous light gray layer. An RT-implanted fin of 12nm CD was completely amorphous while a 32nm CD fin exhibited an amorphous outer layer approximately 7nm thick (Figure 3). These results indicate that a narrow fin would be completely amorphous if its width were less than twice the thickness of the amorphous layer (ta), but would have a c-Si core were its width to exceed 2ta.

To investigate the effect of the spike activation anneal on fin crystallinity, XTEM analysis was carried out on a narrow fin and a wide fin following RT As SDE implant and again after spike anneal (Figure 4). The narrow (6nm) fin had <111> stacking faults near the bottom and was polycrystalline in the top portion, while the 24nm-wide fin was single-crystalline with defects at the top corner. The narrow fin would have been fully amorphous as implanted since its width was less than 2ta, and the wide fin should have had an approximately 10nm c-Si core before the activation anneal. The crystalline core inside the fin plays an important role in recrystallization.

The poor crystallinity of recrystallized fins can be explained by the geometry difference between a planar surface and a fin. In traditional planar devices, the layer amorphized by the SDE implant is planar with its amorphous/crystalline interface parallel to the surface, and recrystallization proceeds by the motion of the interface towards the surface. The recrystallization process is called solid phase epitaxial regrowth (SPER), which occurs at ~550°C and incorporates dopant atoms into the crystal lattice to become electrically active.

The recrystallization of a fin is more complicated than that of a planar device due to its 3D nature and surface proximity. A fully amorphized fin has a top surface and two sidewall surfaces, with the c-Si seed at the bottom of the fin. It has been reported that an amorphous Si atom must complete at least two undistorted bonds to attain SPER. This is not a problem for the <100> surface, but for each atom to form two undistorted bonds, a two-atom cluster is needed at the <110> surface and a three-atom cluster at the <111> surface. This leads to the phenomenon that crystallization occurs most rapidly in the <100> direction, followed by <110> and, lastly, <111>.

It was also reported that micro-twins can form easily on the <111> plane. These results agree with those in Figure 4a, which shows the c-Si after regrowth bounded by <111> stacking faults. The regrowth proceeded only for approximately 5nm from the bottom of the fin. The difficulty in forming two undistorted bonds caused by the Si/native oxide interface at the vertical fin sidewall significantly retarded the SPER. In the absence of SPER, the top portion of the fin in Figure 4a was polycrystalline, seeded from random nucleation in the amorphous Si during the 1020°C spike anneal.

Recrystallization on a wide fin is much easier if there is a c-Si core within the fin. The SPER front propagates from the c-Si core towards the surface as in the case of planar SPER. The fin body can be largely defect-free after recrystallization. However, defects can occur at the corner of the fin due to the proximity of two orthogonal surfaces at the top and the sidewall (Figure 4b).

The abrupt increase in fin conductance at 15nm to 20nm Wfin can be explained by the TEM observation. The low conductance of Wfin of 15nm and below resulted
from the full amorphization of the fin during the RT As⁺ implant and its highly defective state after the spike anneal. For Wfin 20nm and above a crystalline core inside the fin promoted SPER that resulted in much improved crystallinity and therefore much better conductance.

The poor recrystallization after RT implant can be prevented by introducing hot implant for which the substrate is held at an elevated temperature. A 6nm fin remained single-crystalline after hot implant and after spike anneal (Figure 5).

The improvement in fin crystallinity from hot implant is explained by the balance of damage generation and dynamic annealing. The energetic ions damage the Si lattice during the implantation process. This damage ranges from isolated point defects, point defect clusters, and amorphous pockets to continuous amorphous layers. The SDE implant at RT would amorphize the Si fin. Amorphization is the result of a competition between defect accumulation from energetic ion cascades and defect annihilation and out-diffusion from the damaged region.

For a given ion mass and temperature, a threshold dose is required to produce a continuous amorphous layer in single c-Si. The threshold implant dose for the amorphization transition is a function of ion mass, implant temperature, and dose rate. Ion implant produces interstitial-vacancy pairs, the recombination of which is temperature dependent. Rising temperature during implantation makes point defects more mobile and enhances the dynamic annealing and eradication of these defects, which in turn increases the threshold dose for the onset of amorphization. In this way, hot As⁺ SDE implant prevents amorphization of the fins, which improves their crystallinity, leading to reduced junction leakage and parasitic resistance.

A hot implant also changes the amount of de-channeling and defect formation. Substrate amorphization is prevented, which results in a deeper dopant profile. Hence the implant energy may need to be reduced to match the RT implant profile.

**High-Energy, Low-Dose Implant**

A high-energy, low-dose As RT implant was performed on the fins at 5E13 cm⁻² dose, 45keV energy, 20° tilt angle, and 90° twist angle relative to fin orientation. Amorphous pockets were seen on a narrow (8nm) fin (Figure 6a). The 1020°C spike anneal did not fully recover the fin crystallinity, and a defective region was seen at the bottom of the implanted region (Figure 6b).

Hot implant was carried out on 8nm fins at the same implant dose, energy, and tilt angle. The fins were single-crystalline following hot implant (Figure 6c) and after spike anneal (Figure 6d), demonstrating hot implant’s effectiveness in preventing defect formation.

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**Figure 5.** Hot SDE implant enabled single-crystalline 6nm fin (a) following implant and (b) after spike anneal.

**Figure 6.** 8nm-wide fin after high-energy, low-dose RT implant. (a) As implanted and (b) after spike anneal. Similar fin after hot implant. (c) As implanted and (d) after spike anneal.
CONCLUSION
As⁺ SDE implants on fins at different substrate temperatures were characterized by resistance and junction leakage measurements, and by TEM analysis. A narrow fin was completely amorphized by the RT implant, and the crystallinity could not be restored during spike anneal as the Si single crystal seed was at the bottom of the fin and the SPER was severely retarded by fin sidewall surface proximity. A wide fin retained an inner crystalline core following RT SDE implant, which served as seed for recrystallization during spike anneal. Hot implant prevented amorphization of narrow fins during SDE implant by raising the substrate temperature and thereby increasing the threshold dose for amorphization. A 6nm-wide vertical fin remained single-crystalline after hot As⁺ SDE implant and after spike anneal. The hot implant improved narrow fin conductance fivefold and junction leakage more than tenfold.

Halo implants were also characterized on narrow fins. RT As⁺ halo implant produced amorphous pockets; a defective region remained after spike anneal. Narrow fins remained single-crystalline following both implant and anneal when hot As⁺ halo implant was used. Thus, hot implant has demonstrated effectiveness in controlling implant damage and optimizing the doping level in very narrow CD FinFET structures.

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PROCESS SYSTEMS USED IN STUDY
Applied Varian VIISta® 900XPT Medium Current Implant
Applied Varian VIISta® Trident High Current Implant
Plasma Doping of High Aspect Ratio Structures

As semiconductor device technology rapidly transitions to 3D structures, doping specific regions of these devices to enable reliable electrical characteristics presents a unique high-value problem. Doping high aspect ratio (HAR) structures uniformly and with reliable repeatability poses a major challenge for device manufacturers, particularly in the advanced memory and CMOS image sensor technology spaces. Plasma doping offers an effective solution that will aid in commercializing these emerging architectures.

CMOS technology scaling limitations have led to the emergence of vertically integrated cells, which leading-edge chipmakers are already introducing into mass production.[1] These low-power, high-performance devices are likely to be more widely adopted as they facilitate scaling and become less costly.[2,3] In the case of NAND flash memory, chip manufacturers are aggressively pursuing various approaches to 3D fabrication and some are already in pilot production. Many challenges are associated with these new devices, including new transistor architecture, storage mechanisms, and gate fabrication. Each case involves HAR structures that may require doping to improve or even enable device operation. Meanwhile, scaling is driving CMOS image sensor device challenges in pixel-to-pixel isolation, dark-current reduction, and noise reduction.[4-6] This article reports the inherent advantages of plasma doping as an enabling technology for optimizing doping in these challenging HAR structures.

SAMPLE PREPARATION

To evaluate plasma doping performance, HAR Si trench structures were fabricated and then doped using PH3-based or BF3 plasma. Next, they were subjected to a post-implant process flow designed to mimic a typical PR or mask removal. Wet chemistry (SPM/SC1) was used and activation anneal performed prior to analysis. Transmission electron microscopy (TEM) was used to verify the surface response and poly-Si gap fill to examine voiding between trenches (Figure 1a). Completed structures (Figure 1b) were analyzed using a SIMS technique that averages the dopant concentration over several features as the SIMS spot size is larger than the features of interest.

Figure 1

(a) Preparation process flow.
(b) Completed HAR trench.
RESULTS AND ANALYSIS

Study results showed promise in current memory and CMOS image sensor applications. They also indicate the potential for proliferating plasma doping to anticipated future applications.

Memory

As NAND flash memory technology scales, 2D memory will reach fundamental physical limitations as it approaches the 10nm node, giving rise to several new challenges. In particular, the floating gate 2D NAND cell will transition to a 3D NAND in which the cells are stacked vertically. Effectively doping the cell sidewall of the resulting HAR channel is one of the major challenges this change poses.

The stacked memory cells may number 24, 32, or more as the technology scales (Figure 2a). The channel region must not only be doped at a precisely controlled concentration; it must be uniformly doped along the entire length of the channel to avoid threshold voltage variation across the device.

Figure 2. 3D memory cell structure doping.
(a) HAR channel doping region.
(b) HAR SIMS data with dose sensitivity and
(c) HAR SIMS data with energy sensitivity.

Figures 2b and 2c depict uniform doping along the HAR trench with doping concentration on the order of e18 to e19 as a function of the requested dose. The higher dopant concentration at the bottom results from the unobstructed line of sight that facilitates both ions and neutrals reaching the bottom of the trench. These data also demonstrate the potential benefit of plasma doping for HAR staircase contacts in which a high, shallow concentration of dopant ions may be required to improve contact resistance.

The flexibility to tune the sidewall doping concentration as a function of various input parameters is a key feature of the plasma doping approach. Alternatives, such as traditional ion implant, will be limited by the dimensionality of a HAR structure and in-situ doping, using low-pressure CVD for example, may be limited by the required dopant concentration and placement of the dopant species into the substrate at a specified depth. In addition, plasma doping of the channel employs low implant bias and can operate at different plasma densities to tune the deposition and residual damage responses.

CMOS Image Sensors

With the continued growth of the CMOS image sensor market, the demand for better resolution and pixel growth continues to push the image sensor manufacturers. A critical challenge affecting this segment is the requirement to reduce dark current while scaling image sensor technology. As shown in Figure 3, plasma doping is one approach to reducing dark current.
Conventional ion implantation approaches for shallow trench isolation fabrication may produce excessive residual implant damage, which degrades the device by enhancing noise levels and dark current. Implant damage is reduced when using plasma doping as this method employs lower energy and delivers shallower, surface-rich sidewall implantation of low-mass species.

As deep trench isolation (DTI) processes gain traction in the market, crosstalk suppression will add to the challenges cited above. DTI will use HAR trenches to isolate the pixels. Plasma doping offers a potential means of passivating sidewalls with a near-surface, low-damage, dopant-rich process.

**OPTIMIZING HAR PLASMA DOPING**

**Process Mechanisms**

To better tune and refine the plasma doping process, the multiple mechanisms involved must be thoroughly understood. Figure 4 describes the four potential mechanisms that are purported to be critical components for doping of HAR structures.

Based on the results shown in Figures 2b, 2c, and 3b, a clear relationship exists between requested dose or energy and the resultant sidewall dopant concentration. In each case, increasing the energy increases the sidewall doping concentration. These responses point to contributions from the different mechanisms shown in Figure 4, which may be dominated mostly by one mechanism or a cross-product of several. By increasing implant bias energy, higher ion energy in the co-implant carrier gas acts to “knock” the dopant species into the substrate. The angular implant component is also increased, because the energetic component is higher. This enhances the probability that a given ion, regardless of incident angle, will penetrate the substrate.
Plasma Doping

Figure 5. Example multi-setpoint RF capability and DC biasing for HAR doping.

The deposition and thermal drive mechanism is enhanced when plasma doping is followed directly by anneal without an intervening cleaning step. In this case, dopant remains on or near the surface and acts as a source during the subsequent processing steps. The dopant concentration in the sidewall may be enhanced by the in-diffusion of dopant deposition from the surface into the substrate. Such an approach is possible when a hard mask (oxide/nitride) is used, but is not compatible with a PR strip process.

In addition to the data shown in this article, which can be supported by the mechanisms cited above, attempts to model the plasma doping behavior are underway that will advance understanding of these mechanisms and make possible further optimization of these processes.

System Innovations
The plasma doping system used in the above studies allows for independent control of bias (implantation) voltage and radio frequency (RF) plasma generation. The bias voltage is operated using a pulsed DC (direct current) method, enabling very accurate and adjustable pulse timing. For RF plasma generation, a multi-set point RF function allows the RF pulse to be independently manipulated as a function of DC pulse timing. The RF pulse can be adjusted over multiple time periods along with the RF power level in each period.

Figure 5 illustrates the system’s separate mechanisms for modifying RF plasma and pulsed DC bias. Such independent parameter tunability makes it possible to change the timing and RF power level during the bias pulse ON or OFF time. This flexibility, in turn, enables control of deposition and sputter during the doping process, which is critical for meeting device challenges arising from different process integration flows, surface conditions, and feature sizes.

CONCLUSION
The effectiveness of plasma doping in HAR structures has been demonstrated for several 3D device applications. Addressing the doping challenges that 3D structures pose and optimizing the appropriate doping processes requires precise control of the plasma conditions and in-depth understanding of doping mechanisms. As device technologies scale and performance challenges grow, plasma doping technology holds promise for solving future high-value problems.

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PROCESS SYSTEM USED IN STUDY
Applied Varian VIISta® PLAD Ultra High Dose Implant
As planar CMOS device scaling continues, optimizing ultra-shallow junction (USJ) dopant activation and leakage is increasingly challenging. Integrating anneal technologies can mitigate the difficulty. Boosting dopant activation while preserving junction profile and depth is a fine balance strongly influenced by stabilization temperature. The low stabilization temperature of laser millisecond (msec) anneal prevents formation of dopant-deactivating interstitials, preserves junction depth, enhances activation by the following spike anneal, and leads to higher transistor drive current.

Junction optimization is one of the key challenges in producing advanced CMOS devices as it is essential to minimize the parasitic resistance of the device and fully realize the drive current available from advanced transistors. Device scaling requires abrupt USJ with high dopant activation while maintaining low junction leakage. Msec anneal was initially introduced as a means of boosting dopant activation with minimal diffusion. Spike annealing is the hallmark of shallow junction engineering, because of its ability to both activate dopants and control diffusion. However, no consensus has been reached on integrating msec anneal with spike anneal. This article explores the effects of anneal sequences (msec anneal followed by spike anneal and vice versa) and demonstrates that stabilization temperature of the msec anneal plays a significant role in dopant activation.

**EXPERIMENTAL STUDIES**

**Stabilization Temperature**

During the msec anneal, temperature stabilization (which is essentially the wafer pre-heat performed as a single- or multi-step process) is required prior to jumping to the final high temperature (Figure 1). This stabilization is critical for improving within-wafer uniformity and avoiding wafer breakage. The actual stabilization temperature depends on the anneal system technology and application. In general, flash-lamp msec systems require higher stabilization temperatures than laser anneal systems. In this study, experiments were conducted to determine the effects of stabilization temperature on dopant activation.

PMOS source/drain extension (SDE) dopants were implanted (with zero degrees tilt) into blanket n-type <100> Si wafers at -100°C. The implant sequence consisted of germanium (12keV, 5E14/cm²) followed by carbon (3keV, 5E14/cm²) and boron (0.4keV, 1E15/cm²). Implant conditions were designed with a cryogenic implant temperature of -100°C, germanium pre-amorphization implant, and carbon co-implant to capitalize on the
physics of implant damage engineering for boron dopant activation and profile control in the USJ. Spike anneals with peak temperatures ranging from 700°C to 950°C were applied to simulate various stabilization temperatures. Post-anneal sheet resistance ($R_s$) was measured by a high-resolution, four-point Capres microprobe. Secondary ion mass spectroscopy (SIMS) data were analyzed to evaluate the junction profile and dopant activation.

As shown in Figure 2, $R_s$ data at different spike temperatures are normalized by the 700°C condition. $R_s$ increases as spike temperature rises, and reaches a maximum at 850°C, which is consistent with previous studies. The rise in $R_s$ is attributed to dopant deactivation. Si interstitials are created during implants and can diffuse back to the implanted region and form boron-interstitial clusters (BICs) during post-implant anneals. BIC formation, which depends on the anneal temperature, makes the boron dopants electrically inactive. Intermediate temperatures (800-900°C) show the highest $R_s$ linked to high BIC formation and thus should be avoided at the stabilization step during the msec anneal to maximize dopant activation. Once BICs are formed, a much higher thermal budget is required to recover dopant activation by dissolving them. But higher thermal budgets produce deeper junctions by increasing diffusion rates. Therefore, a low stabilization temperature is essential for achieving high dopant activation while maintaining the USJ profile.

Anneal Sequence
In this study alternating flow sequences were explored between spike and msec anneals to identify ideal conditions for junction annealing. PMOS SDE cryogenic implants were applied under the same conditions as described above.

Figure 3 plots the $R_s$ data of various anneal conditions, normalized by the msec 1200°C condition, while Figure 3b plots SIMS results of corresponding anneal conditions. Junction depth ($X_j$) is taken at 5E18cm⁻³, and the normalized $1/(\text{median } R_s \cdot X_j)$ is plotted in Figure 4, which reflects dopant electrical activation.

Of all the anneal conditions, msec 1200°C has the lowest $R_s$, while spike 750°C has the highest—approximately 70% higher than that of msec 1200°C, which cannot be explained by the subtle difference in $X_j$. Meanwhile, the anneal sequence results in clear differences. $R_s$ is approximately 50% lower after the msec + spike sequence despite the shallower junction of this sequence. This $R_s$ difference is related to dopant activation.
In the spike and spike + msec cases, BICs are formed at the intermediate spike temperature, adversely affecting dopant activation. Subsequent 1200°C msec anneal can improve Rs only to some extent, at the cost of a deeper junction. Complete dissolution of BICs requires even higher thermal budget, which inevitably leads to a deeper junction.

On the other hand, in the msec and msec + spike scenarios, the msec stabilization temperature is only 400°C, which is low enough to prevent Si interstitials from diffusing. The fast msec anneal temperature ramp-up and high peak temperature are able to annihilate the Si interstitials before they form clusters, avoiding dopant deactivation from occurring in the first place. Although msec anneal is effective in dissolving Si interstitials, a subsequent spike anneal is still recommended to repair residual implant damage. Clearly, a low stabilization temperature affords substantial dopant activation benefits.

Experiments with spike temperatures of 800°C and 900°C were also performed and the same trends were observed.

**Validation of Results**

The anneal sequence effects were validated on device wafers. Gate-first transistors were fabricated, with the shortest gate length being approximately 50nm. Source/drain (S/D) activation annealing was performed on splits. Figure 5 compares the $I_{\text{dsat}} - I_{\text{off}}$ curve for the split subjected to conventional spike 1050°C anneal vs. the split processed with a msec 1200°C followed by spike 1050°C. Clearly, at the same $I_{\text{off}}$ (100nA/µm), the $I_{\text{dsat}}$ of the msec + spike split is more than 10% higher.

In addition, Miller capacitors were fabricated to characterize the S/D dopant lateral out-diffusion under various anneal conditions. Figure 6 shows the derived $L_{\text{ov}}$ (gate-S/D overlap length) for both spike 1050°C and msec 1200°C + spike 1050°C splits. Essentially, both anneal conditions lead to the same $L_{\text{ov}}$, implying that the addition of msec anneal does not cause additional dopant lateral out-diffusion. Thus, the gain in $I_{\text{dsat}}$ can be attributed to superior S/D dopant activation, rather than to the shorter electrical gate length.
CONCLUSION
A low msec stabilization temperature is crucial for achieving high dopant activation while preserving an abrupt dopant profile and USJ depth. The msec + spike scheme also exhibits significantly higher dopant activation than the spike alone and spike + msec approach, which is attributable to the substantial annihilation of BICs. These results were validated on gate-first transistors, which exhibited higher $I_{D_{sat}}$ for the msec + spike sequence than for the spike-only process.

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