Serving Semiconductor Manufacturers Worldwide With Enabling Process Technology

In This Issue:

• Solid State Doping of 3D Structures
• Novel Process for Conformal TSV Liner
• Fully Characterized GST CMP Process
• Source Mask Optimization Using Aerial Imaging

Solving Critical Transistor Scaling Challenges
The formidable challenges posed by scaling continue to drive innovations in our industry. The benefits of smaller dimensions, higher performance transistors, more efficient on-chip and chip-to-chip interconnections, are felt directly by the consumer in more capable and lower power electronic devices. Recent innovations in lithography, new transistor materials and processes, and novel packaging methods are some of the key drivers fueling the semiconductor technology treadmill. With Semitool joining our packaging and interconnect portfolio of products, we are now impacting the most critical areas of the IC industry—transistor and chip packaging—in addition to our seminal portfolio of enabling products. In this issue of the Nanochip Technology Journal, we report on our most recent developments that focus on these challenges.

Controlling leakage impacts both device performance and low-power functions, making it one of the most significant issues for transistor scaling. To contain leakage, aggressive source/drain and junction techniques have been widely investigated by the industry. At Applied, we have enabled a novel nickel silicide formation technique using our new laser-based millisecond anneal technology that dramatically reduces junction leakage in aggressively scaled devices. These results have been verified in several studies and presented at IEDM. Please take the time to read about this exciting breakthrough on page 6.

We also report on several advances for emerging Through Silicon Via (TSV) applications that vertically interconnect stacked chips to deliver greater performance in a smaller form factor. A critical challenge for TSV integration has been electrically insulating the near-vertical sidewalls of high aspect ratio vias. Our new and unique CVD process, optimized for via-first and via-middle integration schemes, is an enabling technology that delivers a highly conformal and robust liner film. To address another challenge involving doping vertical surfaces, we’ve developed an SACVD process that demonstrates controllable surface concentrations with high activation levels as an alternative to high energy ion implantation.

Rounding out this issue, we present a study on a CMP process for phase change materials and report on a joint effort with IMEC to demonstrate electrically functional SRAM cells using EUV lithography for contact and metal 1 levels.

I trust you will find this issue of great interest. The articles in this issue are a reflection of the technical and product innovations of our dedicated engineers.

**Cover Feature:** Solving Critical Transistor Scaling Challenges

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Front cover: A new millisecond anneal (MSA) system solves critical transistor scaling challenges to enable faster, lower power consumption devices. Targeted for creating the sensitive nickel silicide (NiSi) transistor contact layers in 45nm and beyond logic chips, this advanced laser-based system can enhance drive current and reduce gate leakage by an order of magnitude.

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Conformal Oxide Liner Technology for High Aspect Ratio TSVs

A highly conformal insulating liner has been developed for FEOL through-silicon via (TSV) integration. The liner demonstrates step coverage of 50-90% on TSV structures with high aspect ratios (HAR) up to 11:1, as well as excellent adhesion to metal barriers and robust electrical performance.

Keywords: TSV Integration, Oxide Liner, SACVD, Via-first, Via-middle

Vertical or 3D integration can enable improved functionality by integrating devices with incompatible process flows such as memory and logic. Recent announcements by several semiconductor companies about working prototypes of stacked memory[1] or DRAM on logic stacking[2] suggest an accelerated effort to bring this technology to market. The primary technology drivers for 3D integration have been extensively published[3] and are centered on improved electrical performance, lower power consumption, and form factor reduction.

A simple process flow for TSV creation is shown in Figure 1. It involves etching the silicon to create the via, depositing a dielectric liner for insulation, depositing a metal barrier and Cu seed using PVD-based processes, and finally, electroplating with Cu to fill the structure.

Front end of line (FEOL) TSV integration schemes can be classified as via-first, if the TSV is formed before the transistor; or via-middle, if it is fabricated after the transistor. In back end of line (BEOL) TSV schemes, also called via-last, the vias are created after the Cu interconnect. Depending on where in the process flow the TSVs are created, there will be differences in the final aspect ratio and allowable thermal budget. Via-first TSVs essentially have no thermal budget requirement, via-middle TSVs have an upper limit of 400°C, and via-last processing must typically remain below 200°C. This is because via-last requires the wafer to be bonded to a glass substrate, with the glue layer becoming the limiting factor.

This study focuses on the FEOL TSV dielectric liner that is deposited before the metal barrier in via-first and via-middle schemes where thermal budgets are in the range of 400°C or higher. The primary purpose of the dielectric is to electrically isolate the individual TSVs, so good electrical performance (dielectric breakdown, leakage) is paramount. Since these TSVs have CDs from 5–50μm and depths up to 100μm, adequate dielectric coverage on the sidewall is critical. In addition, it is important that the resulting dielectric film profile is conducive to subsequent metal deposition. The plasma-based metal barrier and seed deposition steps are inherently line-of-sight so cannot directly deposit uniform coatings on highly reentrant structures. These and other key requirements for the oxide

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
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<tbody>
<tr>
<td>Thermal Budget</td>
<td>Via-first - no limitation</td>
</tr>
<tr>
<td></td>
<td>Via-middle - ≤400°C</td>
</tr>
<tr>
<td></td>
<td>Via-last - ≤200°C</td>
</tr>
<tr>
<td>Step Coverage</td>
<td>&gt;50% over entire sidewall</td>
</tr>
<tr>
<td>Film Thickness</td>
<td>2-10kÅ on sidewall</td>
</tr>
<tr>
<td>Adhesion</td>
<td>Good adhesion to downstream</td>
</tr>
<tr>
<td></td>
<td>barrier layer (TaN/Ta/Ti)</td>
</tr>
<tr>
<td></td>
<td>Good adhesion to Si</td>
</tr>
<tr>
<td>Productivity</td>
<td>High throughput</td>
</tr>
<tr>
<td></td>
<td>Low cost of ownership</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>&gt;7MV/cm</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>k≤4.3</td>
</tr>
<tr>
<td>Film Roughness</td>
<td>Smoother film desired</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>&lt;2nA/cm²</td>
</tr>
</tbody>
</table>

Table 1. Key requirements for TSV dielectric isolation liner.

Figure 1. Simple process flow for Cu-filled TSVs.
Conformal TSV Liner

liner dielectric in FEOL TSVs are shown in Table 1.

Undoped SACVD using O₃/TEOS-based chemistry is an established process technology being considered as a solution for FEOL TSV liners since it meets both the coverage and electrical isolation specifications within the required thermal budget. A further benefit of this process is its ability to smooth out surface roughness in cases where the preceding dry etch process has left some scalloping on the silicon sidewalls. As long as the dielectric liner is thicker than the depth of the trench sidewall scallop, a smooth interface can be established for metal liner and seed deposition.

Experimental Work and Results

O₃/TEOS-based films were deposited in an SACVD reactor which was tailored to deposit HAR liners for TSV applications. The chamber contains a heater capable of providing wafer temperatures from 400-600°C, a showerhead for optimal control of TEOS/O₃ mixing, and an in situ RF plasma generation capability for sealing the film. Films were deposited in the sub-atmospheric pressure regime and controlled using a throttle valve downstream. Liquid TEOS is vaporized and introduced into the chamber using nitrogen as a carrier gas, then mixed with O₃ above the wafer.

Sidewall Coverage

Sidewall coverage, defined as the ratio of the thickness on the sidewall to the thickness in the field area, was measured for a variety of via openings and via depth dimensions (Figure 2). Deposition of a highly conformal dielectric liner was achieved for a range of TSV dimensions (Figure 3).

Step coverage for O₃/TEOS films is dependent on the cleanliness of the TSV structure, taper angle, aspect ratio and the presence of any materials on the field that would retard nucleation and growth on the field, while promoting growth in the Si trench. It is essential that the TSV structures are completely cleaned of any polymeric etch residues prior to liner deposition as these processes are sensitive to the underlying substrate and have an incubation time before film growth proceeds.

This mechanism can actually be turned into an advantage by engineering the TSV structures with materials on the field and the upper part of the via sidewall to create more tapered oxide liner profiles that would support subsequent PVD deposition.

Figures 4 and 5 show the step coverage of the TSV film as a function of aspect ratio and critical dimensions (CD) respectively. Step coverage of the film decreases monotonically as a function of aspect ratio, but still shows excellent performance of >50% for TSVs with aspect ratios as high as 11:1. The sidewall coverage measurements were made at the midpoint of the TSV depth.

A sharp decrease in step coverage for TSVs with CDs below 10μm can be seen in Figure 5 suggesting a constrained flow of chemical reactants in narrower structures. As CDs increase to 50μm, we see that sidewall coverage as high as 90% can be achieved. Differences in taper were not accounted for in this study.

Adhesion

Adhesion of the dielectric liner to the Cu metal barrier is critical for good electrical properties and also to prevent delamination during downstream processes such as CMP. Cu barriers that have been of interest for TSV are the traditional BEOL materials.

Figure 2. Excellent sidewall coverage was achieved over a range of TSV CDs and aspect ratios.

Figure 3. SEM images show excellent sidewall coverage from the O₃/TEOS process over a range of TSV dimensions.
Conformal TSV Liner

such as TaN and Ta, as well as Ti for its lower overall cost. All three metal barriers were evaluated in this adhesion study.

Interfacial strength measurements were carried out using the four point bend method.[4] The samples used were multilayer thin film stacks consisting of the TSV liner (50nm) deposited on a bare Si wafer. This was followed by the deposition of various Cu metal barrier interfaces, including TaN, Ta and Ti, using PVD. Samples were prepared using the DPN-free (dicing, polishing and notching free) method in which two silicon chips of 40x40mm cut from the wafer are bonded face-to-face and cured with EPO-TEK 375 epoxy with a known maximum strength. The bonded specimen was cleaved into ~5x40mm beams with lateral edges along the <010> lattice direction to ensure exact parallel alignment of the <100> directions of the two chips and smooth, defect-free sidewalls. The multilayer thin film test stacks include different metal barriers (Figure 6). The test was carried out by applying a load to the sandwiched specimen for bending at a constant displacement rate of 0.1μm/s.

The TSV stack shown in Figure 6 delaminated consistently at the BLOk/epoxy interface, rather than at the TSV liner/Cu metal barrier interface, with adhesive fracture energy, $G_c$, ranging from 10-50 J/m$^2$. Due to its strong interfacial strength, quantitative $G_c$ measurements for the TSV liner/Cu interface were not obtained. Nevertheless, $G_c$ for this interface can be inferred to be $>5$J/m$^2$, which is strong enough to withstand the stress of subsequent packaging and reliability testing.

Cap to Prevent Moisture Absorption

One of the concerns with O$_3$/TEOS films deposited at ~400°C is moisture affinity. Moisture absorption takes place rapidly, changing the film structure, reducing stress, and increasing the dielectric constant of the material. The liner will typically go through a degas step to remove all residual traces of moisture before Cu barrier deposition. If moisture is present in the dielectric films, there is a potential for metal barrier oxidation that can affect electrical performance and adhesion.[5] To prevent moisture absorption of the dielectric liner, aPECVD oxide capping layer can be deposited in situ to create a hermetic seal on the O$_3$/TEOS film.

Figure 7 shows stress as a function of time for O$_3$/TEOS based films deposited at 400°C. The uncapped film shows stress decreasing with time as the film absorbs moisture and relaxes, but with a PE oxide cap applied in situ, the film retains stress over 30 hours. FTIR analysis confirms that the moisture peak of the as-deposited film increases for up to 48 hours (Figure 8). To ascertain the optimum cap thickness, dif-

![Figure 4. Dielectric liner step coverage as a function of aspect ratio for TSV structures.](image)

![Figure 5. Dielectric liner step coverage as a function of CD opening.](image)

![Figure 6. Stacks used for adhesion testing with different metal barriers.](image)

![Figure 7. Application of an in situ PECVD oxide capping layer prevents relaxation of the SACVD liner from moisture absorption.](image)
ifferent PE cap thicknesses were applied to the as-deposited film. As can be seen from the FTIR plots, the water absorption peak is completely suppressed with even a 50Å cap thickness.

**Degas Process Optimization**

To understand the extent of moisture absorption prior to metal barrier deposition, a quadropole mass spectrometer was attached to the degas chamber to record the time-flight partial pressure (TFPP) curves. The degas chamber used provides fast temperature ramp rates through heater and lamp heating and pump/purge cycles during processing to efficiently remove moisture.

Figure 9 illustrates the typical characteristic H2O TFPP curves obtained during the degas process, comparing capped and uncapped films. The degas temperature was set at 400°C and the pressure was varied from 0.5–8.0Torr in the purge and hold (degas) steps, respectively, with carrier gases Ar and N2. H2O out-gassing decayed exponentially with the degas time, a partial pressure in the 10-11A range being reached in approximately 10 minutes. With a thin, 100Å PE oxide cap, that pressure is reached in less than one minute. Increasing the thickness of the PE cap to 1000Å showed no benefit of reduction in moisture absorption, which is consistent with the FTIR results that showed a thin 50Å PE cap provided an effective hermetic seal.

**Electrical Testing**

The key electrical parameters for a TSV liner, breakdown voltage (V_{bd}) and leakage current, were characterized using MOSCAP structures (Figure 10). The test was performed using two terminal measurements. The device under test was fabricated with a large Al cap area (0.1cm²) to reduce edge effects. The plate temperature was allowed to stabilize at 150°C prior to loading the first wafer and a 5 minute wait time was allowed after each wafer was loaded. Bias voltage sweep was applied with a shielded tungsten probe tip while the hot plate was grounded. Negative bias was forced from the probe tip to characterize the leakage and breakdown behavior. Data was collected at 1V intervals with 0.2 second delay between measurements (Figure 11).

The 400°C O3/TEOS baseline process film was used for comparison with the capped process sample. Breakdown voltage and current densities were measured for these two samples (Table 2).

High insulation capability for the TSV liner is necessary to ensure correct device function in high voltage applications. Both capped and uncapped liners achieve V_{bd} >8MV/cm which is high enough to withstand the TSV application requirements. However, higher leakage current was observed on the uncapped process as compared to the capped film and this can be attributed to moisture uptake in the uncapped process upon exposure to the ambient atmosphere. The 50Å cap thickness on the samples was sufficient to provide

<table>
<thead>
<tr>
<th>Parameter @150°C</th>
<th>400°C O3/TEOS</th>
<th>400°C O3/TEOS + In Situ PE Cap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage Current (NA/cm²@1MV/cm)</td>
<td>&gt;10</td>
<td>&lt;1</td>
</tr>
<tr>
<td>Breakdown Voltage (MV/cm)</td>
<td>&gt;8</td>
<td>&gt;8</td>
</tr>
</tbody>
</table>

Table 2. The addition of a cap layer greatly reduces leakage current without affecting V_{bd}.
Conformal TSV Liner

Improved leakage. Figure 11 shows that the $V_{bd}$ curve for the O$_3$/TEOS film with a 50Å PE cap has excellent leakage performance and a sharp breakdown characteristic.

Conclusion

A highly conformal insulating liner has been developed for FEOL TSV integration using O$_3$/TEOS chemistries. Step coverage of 50-90% has been demonstrated on a variety of different TSV structures and can be modulated by using a different hard-mask material in the field. Step coverage typically decreases with increasing aspect ratio and decreasing CD, but >50% can be obtained for aspect ratios as high as 11:1 and CDs as small as 4μm. Adhesion tests indicate excellent adhesion with Si, TaN/Ta bilayers, Ta and Ti. An in situ PE cap has been developed to hermetically seal the as-deposited film, preventing moisture absorption, leading to decreased degas times and improved electrical performance.

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A two-step anneal process for 32nm NiPt silicide formation was developed to improve source/drain (S/D) resistance, resistance uniformity and reduce device leakage. A lower temperature first step reduced physical defects while a higher temperature millisecond anneal (MSA) second step improved NiSi roughness, suppressed NiSi agglomeration and reduced NMOS nickel piping defect formation. The optimized process improved S/D resistance and increased CMOS drive current by 4% on NMOS and 3% on PMOS transistors.

Keywords: NiPt Silicide, Rapid Thermal Processing, Millisecond Anneal, NiSi, 32nm

Nickel silicide (NiSi) is used to create low resistance ohmic contacts between CMOS transistors and interconnects. Critical dimension scaling and shrinking geometries are demanding shallower junctions and correspondingly thinner NiSi layers. The challenge is to fabricate these thinner areas while maintaining low contact resistance and low current leakage.\(^{[1]}\)

Nickel silicidation typically involves two separate rapid thermal processing (RTP) anneal steps. The first anneal (RTP-1) is typically performed at a low temperature (220–300°C) to drive Ni diffusion into the underlying Si to form predominantly \(\text{Ni}_2\text{Si}\). The key challenge during this step is the formation of a thin, metal-rich silicide layer while controlling the silicide-Si interface quality. Excessive nickel diffusion must be avoided, since short channel nickel “pipes” or “spiking” defects can form and cause current leakage. A wet process is used to selectively remove unreacted metal.

The second anneal (RTP-2) is typically performed at a higher temperature (400–500°C) and transforms the nickel silicide from the higher resistance \(\text{Ni}_2\text{Si}\) phase into the low resistance NiSi phase. The key challenge during this step is achieving complete and uniform phase transformation without NiSi agglomeration (Figure 1). Lower temperature anneal has been reported to reduce nickel piping and leakage\(^{[4]}\) while the higher temperature anneal process has the potential to raise the Schottky barrier height of the silicide-Si interface layer. This can reduce contact resistance\(^{[5]}\) and lead to better CMOS drive current \((\text{I}_{\text{on}}/\text{I}_{\text{off}})\). MSA can provide a higher temperature (>800°C) to drive the NiSi phase transformation with a low thermal budget. This can suppress thermal energy-induced NiSi agglomeration or further nickel pipe diffusion. The

Figure 1. SEM images show (left) normal NiSi formation and (middle) NiSi agglomeration; a TEM image (right) show NiSi agglomeration in cross-section.

Figure 2. 32nm nickel silicidation process flow.
mechanism of NiSi agglomeration, driven by texturing and interface energy reduction during conventional annealing, may be different in the MSA case due to the much higher temperatures and tremendous compressive stresses induced at the surface during the anneal.[6, 7]

In this study, a lower temperature RTP-1 process was characterized to determine its effect on NiSi and piping defect formation. An MSA RTP-2 process was explored for low resistance NiSi formation. Lastly, the impact of an integrated anneal process combining a lower temperature RTP-1 and higher temperature RTP-2 by MSA on CMOS device performance parameters was measured.

Experimental Work

Both blanket and patterned wafers were prepared using a 32nm process flow (Figure 2). First, native silicon dioxide on the wafer was removed and Ni(Pt)/TiN metal deposited. The RTP-1 anneal was performed under different conditions to form the nickel-rich silicide (Ni$_2$Si) layer. A wet selective etch process in a batch spray processor was used to remove unreacted metal. The RTP-2 step was performed using the baseline RTP-2 spike anneal under several MSA process conditions to form the final NiSi.

A scanning laser-based MSA system was used for the RTP-2 step, providing ~10$^5$ °C/s temperature ramp rate to a peak temperature of 780-980°C with temperature accuracy of ±5°C and repeatability of ±2°C.

On blanket wafers, after the RTP-2 process, sheet resistance ($R_s$) was measured by a four-point probe. SEM, TEM and XRD were used to characterize NiSi agglomeration and microstructure. The RTP-2 MSA process window was determined using these results.

On 32nm patterned wafers, after the RTP-2 process, NiSi agglomeration behavior was measured using a defect inspection system and TEM. The wafers then continue with CMOS integration to form tungsten contacts. After planarization (W-CMP), nickel piping defects were characterized using an electron beam brightness voltage contrast (BVC) count.[8] CMOS device electrical performance was measured by a multi-point electrical probing station after metal-1 layer formation.

Results and Discussion

Sheet Resistance on Blanket Wafers

Two groups of process conditions were explored: baseline RTP-1 soak anneal (T1 220-300°C) and a lower temperature condition (T1-40°C), combined with an MSA RTP-2 anneal with temperatures from 780-980°C. It is observed that the lower temperature RTP-1 results in higher $R_s$ compared to the baseline RTP-1 temperature (Figure 3). Because the silicide

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**Figure 3.** MSA results show the process gives consistent results over a wide temperature range. Above 950°C, phase transformation to NiSi$_2$ occurs, raising $R_s$.

---

**Figure 4.** GIXRD spectra from different RTP-1 and RTP-2 conditions show that phase transformation is strongly correlated with RTP-2 temperature.
thickness is controlled to the same level by adjusting the soak annealing time, this $R_s$ shift is considered to be dominated by the NiSi phase composition.

Stable $R_s$ over a wide MSA temperature range up to 950°C was also observed on both RTP-1 cases, indicating that no significant NiSi phase change or agglomeration takes place. When the MSA RTP-2 temperature exceeds 950°C, $R_s$ begins to increase dramatically, indicating that either NiSi agglomeration is taking place or that the NiSi is beginning to undergo further phase transformation to more resistive NiSi$_2$.

**NiSi Agglomeration**

TEM micrographs of NiSi films of equal thickness produced by the processes summarized in Table 1 show the impact of process conditions on surface roughness (Figure 5). Process B shows better NiSi film roughness (16%) compared to the baseline process A (33%), suggesting that lowering the RTP-1 temperature can reduce NiSi agglomeration. Process C results in even better NiSi film roughness (<10%), indicating that a lower temperature RTP-1 combined with a higher temperature MSA RTP-2 anneal can further suppress NiSi agglomeration.

**Ni Piping Defect Formation on Patterned Wafers**

Piping defect measurement is performed using a scanned electron beam after tungsten plug fabrication. When a charged plug is in contact with a leaky junction or a leaky polysilicon gate, the electrons from the substrate can neutralize the positive charge, and its SEM image indicates higher brightness. BVC was reported as effective in characterizing the nickel piping behavior.\(^\text{[9]}\)

The lower temperature RTP-1 step combined with MSA RTP-2 produces fewer piping defects (Figure 6). Piping diffusion is mainly driven by the thermal dynamics during the anneal process. Any line defects or stack faults in the atomic structure could, by thermal exposure, allow rapid defect formation and expansion by diffusion. Thus, this result indicates that the MSA RTP-2 has very low Ni secondary diffusion producing a virtually diffusion-free result that suppresses pipe formation.

**Phase Transformation on Blanket Wafers**

Grazing incidence XRD (GIXRD) spectra were recorded for both RTP-1 cases (T1 and T1−40°C), and MSA RTP-2 temperatures in 20°C increments from 880-940°C (Figure 4). The evolution of the NiSi phases with temperature is quite clearly observed, an indication that NiSi phase transformation is strongly correlated with MSA RTP-2 temperature.

This blanket wafer data provided a good starting point for the process conditions to be used on patterned wafers.

**Table 1. RTP process conditions.**

<table>
<thead>
<tr>
<th>Process Split</th>
<th>RTP-1</th>
<th>RTP-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>T1</td>
<td>T2</td>
</tr>
<tr>
<td>B</td>
<td>T1−40</td>
<td>T2</td>
</tr>
<tr>
<td>C</td>
<td>T1−40</td>
<td>MSA (T2 + 400)</td>
</tr>
</tbody>
</table>

Figure 7. NiSi $R_s$ increases with both lower temperature RTP-1 and the use of MSA for RTP-2.
32nm NiPt Formation

Sheet and Source/Drain Resistance on Patterned Wafers

$R_s$ and $R_{S/D}$ were measured on both NMOS and PMOS transistors (Figures 7 and 8). From Figure 7, it is noted that lower RTP-1 in process B results in higher $R_s$ as compared to process A and the MSA RTP-2 further increases $R_s$. This confirms the blanket wafer result (Figure 3). It is believed that the nickel phase composition dominates the sheet resistance behavior at this film thickness (<50nm). This modest increase in $R_s$ is considered an acceptable penalty because it is outweighed by the improvements in defectivity, leakage current and $I_{on}/I_{off}$ performance.

Conversely, $R_{S/D}$ was reduced by the use of MSA (Figure 8). To explain this phenomenon, consider that the electrical current flow in a MOSFET has a series of resistance components, but the silicide resistance only contributes a very small amount compared to the S/D resistances. The overall S/D resistance reduction suggests that the S/D resistance has also been reduced by the high temperature MSA RTP-2 process. This may be attributed to the reduction in Schottky barrier height at the NiSi/Si interface\(^{[10]}\) through reduced dopant deactivation compared to conventional soak and spike anneals.

Device Drive Current

Transistor $I_{on}/I_{off}$ performance using the different RTP processes was measured after metal-1 layer fabrication (Figures 9 and 10). Figure 9 shows that the lower temperature RTP-1 process B has slightly improved drive current on NMOS and no gain on PMOS compared to baseline process A. Figure 10 shows that the process C has resulted in 4% drive current improvement on NMOS and 3% on PMOS, respectively. These results correspond well with the $R_{S/D}$ resistance results shown in Figure 8.

Conclusion

The potential for an improved RTP process using MSA has been demonstrated for 32nm CMOS NiPt silicide formation. The results show that a lower temperature RTP-1 step reduces physical defect formation and a higher temperature MSA RTP-2 step improves NiSi roughness, suppresses NiSi agglomeration and suppresses NMOS nickel piping defect formation. The combined RTP process, applied to patterned wafers, has demonstrated the effective reduction of Ni piping defect by BVC inspection, improved $R_{S/D}$ on NMOS by

![Graphs showing the comparison of drive current for NMOS and PMOS between different processes.](image-url)
5% and 8% on PMOS and increased drive current ($I_{on}/I_{off}$) by 4% on NMOS and 3% on PMOS.

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Conformal Doping
SACVD Process for 3D Structures

To address the challenge of conformal doping on 3D structures, a novel sub-atmospheric CVD-based doping process is proposed to replace conventional high-energy ion implantation methods. The new process demonstrates controllable surface concentrations of greater than $10^{21}$ atoms/cm$^3$ in damage-free junctions as shallow as 6nm, with high activation levels.

Keywords: SACVD, STI, ILD Gapfill, Conformal Doping

To overcome the limitations on drive current and packing density of planar transistors, logic FinFET and DRAM vertical transistor architectures are being developed. However, the need for controlled doping of vertical surfaces highlights an intrinsic limitation of ion implantation. In ion implantation, ionized gas atoms, accelerated by an electric field, impinge on and penetrate the wafer surface, doping the underlying material. By tilting the ion beam, ion implantation can implant the sidewalls of isolated structures or transistor arrays placed on a relaxed pitch, but the inherent line of sight nature of ion beams precludes their use in densely placed transistors.[1] In addition to this technical limitation, tilt-implantation requires multiple implant steps to dope all sides of a device, which increases manufacturing cost.

To address the challenge of conformal doping, a novel implantation method[2] that uses proven sub-atmospheric CVD (SACVD) technology as a source of dopants for thermal in-diffusion and activation is proposed. The new SACVD process, coupled with recent advances in surface preparation and millisecond anneal (MSA), demonstrates controllable surface concentration in excess of $10^{21}$ atoms/cm$^3$ and damage-free ultra-shallow junctions (USJ) with depths as low as 6nm with high levels of activation.

SACVD is a standard method for shallow trench isolation (STI) and inter-layer dielectric (ILD) gapfill that delivers highly conformal coverage with minimal pattern dependence. By introducing additional precursors during deposition, doped oxide films can be readily achieved while maintaining conformality. Doped films containing boron and phosphorous are commonly used, primarily as an oxide fill for interlayer and capacitor dielectrics, gettering layers and masking films. Other dopants such as arsenic can be easily integrated into the SACVD process. A further advantage of SACVD is its proven productivity, defectivity, and process control.

**Experimental Work**

A simple process flow for conformal doping of a logic FinFET structure is shown in Figure 1. Following STI recess formation, the native oxide is removed from the silicon fin using a dry chemical clean to create a pristine silicon surface. Keeping the wafer under vacuum, an SACVD doped amorphous film is then deposited. An MSA is used for dopant thermal diffusion and thermal activation. Finally, the SACVD glass is removed from the fin with dilute hydrofluoric acid. Due to the high etch rate of doped film in the presence of moisture, the doped film can be removed with selectivity of >6:1 for phosphosilicate glass (PSG) and >4:1 for borosilicate glass (BSG) with respect to the STI oxide. The clean to remove native oxide is performed using a dry chemical clean process which provides a highly selective removal of the native oxide without damage to the silicon fin. While in-diffusion can occur with native oxide present, the removal of the native oxide has been found to increase the junction’s surface concentration. While in-diffusion and activation can be achieved through rapid thermal processing (RTP), MSA or a combination of RTP and MSA affords greater control of diffusion depth for shallow junctions.

![Figure 1. Process flow for conformal doping of a logic FinFET structure.](image-url)
used precursors for BSG and PSG depositions respectively. Controlled amounts are introduced into the SACVD reactor along with triethyloxysilane (TEOS) and ozone which form the silicon dioxide film through gas phase intermediaries.

Dopant precursors react with ozone and the resulting gas phase intermediaries and are incorporated into the structure of the growing silicon dioxide matrix as oxide networks. The dopant concentration can be modulated by controlling the ratio of the dopant precursors to TEOS. The chamber pressure—maintained at a constant pressure during film deposition—and the substrate temperature determine the quality and conformity of the oxide film. Substrate temperatures between 200°C and 550°C and chamber pressures as high as 600Torr are possible for deposition of doped amorphous films.

For high doping concentrations, the diffusion coefficient in silicon is no longer a constant as governed by Fick’s diffusion equation of continuum theory, but becomes concentration dependant and hence the atomistic theory of diffusion will prevail. Atomistic theory assumes that the dopant atoms will diffuse by jumping from one site to another only through interactions with native point defects (vacancies and interstitials) in the silicon lattice. This mechanism underlines the need for non-bonded dopant oxides to be abundant on the native Si surface in order to achieve high concentrations of dopant in the silicon after high temperature annealing. As a result, the new doping processes are able to control the interface between the silicon and the doped film.

The SACVD film is deposited in three steps. A thin, <1.5nm layer is deposited on the silicon surface by flowing the dopant source in the presence of ozone or another oxidizer. We describe this thin layer of deposit as the “dopant spike.” A 5-10nm doped glass film is then deposited using ozone, TEOS, and dopant sources followed by a 3-5nm termination layer in which the dopant sources are turned off. This termination layer separates the high concentration doped film from moisture in the environment to avoid the formation of crystalline salts.

The dopant concentration of the amorphous film influences the surface concentration and depth profiles achieved through subsequent anneal. The dopant spike provides a significant enhancement by enabling a high dopant concentration and a different chemical environment at the silicon surface. This enhancement ensures that dopants can readily diffuse and enables surface concentrations in excess of $10^{21}$ atoms/cm$^3$ even with shallow junction depths.

The dopant concentrations in the bulk of the doped glass films were measured by secondary ion mass spectroscopy (SIMS) for thin films (10nm) and by x-ray fluorescence spectroscopy (XRF) for thick films (200nm). Measurements made using the two different techniques correlate well (Figure 2). Dopant concentrations of phosphorus and boron as high as 12wt% and 9wt% respectively were achieved. The phosphorus–doped spike layer was characterized by SIMS (Figure 3). The dopant spike regime had phosphorous concentration peaking at ~11% at the silicon interface and then decreasing to ~7% in the bulk amorphous film. The ability to control the extent of the dopant spike (concentration and time) as well as the dopant concentration in the bulk allows for a wide range of desired surface concentrations at the interface as well as the depth profile.

Conformality

SACVD deposition is a thermal CVD process that uses O$_3$/TEOS chemistry to achieve excellent conformality. Pressures from 200–600Torr allow for a highly conformal film to be deposited in deep trenches with aggressive aspect ratios. The oxide depositions (10–20nm) maintain this conformality even with the addition of dopant precursors. Conformality of the SACVD film was characterized by scanning electron microscopy (SEM) on >6:1 aspect ratio STI structures intended to simulate DRAM vertical gate aspect ratios.
and silicon fins of 30nm width and 85nm height intended to simulate FinFETs.

Sidewall or bottom coverage was defined as the ratio of the thickness on the sidewall or bottom of the structure to the thickness deposited in open areas. High conformality of typically >90% coverage on the STI structure was achieved for both BSG and PSG doped films (Figure 4). Similarly high conformality of PSG and BSG films on the silicon fin structure was demonstrated (Figure 5).

In-Diffusion Studies
Dopants move from the interface of the doped amorphous film to the silicon substrate through solid-state diffusion. Increasing the dopant concentration within the amorphous film provides a reservoir of additional dopant atoms. In addition to SACVD process conditions, anneal time and temperature have a strong impact on the surface concentration and junction depth for diffusion.

Initially, RTP spike and soak anneals in a nitrogen ambient environment were investigated. Anneal temperatures from 900–1,100°C and anneal times from 1.5–60s were tested. While surface concentration could be modulated with RTP anneals, junction depths shallower than 20nm could not be achieved. To achieve shallow junctions, MSA was employed, that allows dwell times of tens of milliseconds. By using short dwell times and higher temperature the junction depth could be controlled while maintaining high surface concentration.

Silicon fins with doped amorphous films were subjected to MSA and assessed by SEM. No change in structure was observed from anneals as high as 1,200°C. This was attributed to the presence of the amorphous doped film, which protects the silicon fin from rounding during the anneal.

Studies of in-diffusion were carried out using SIMS on blanket silicon substrates. Doped glass films with maximum dopant concentration of 12% for PSG and 9% for BSG were deposited following dry chemical clean and dopant spike steps. MSA was performed with 50ms dwell time at 1,200°C. The SACVD film was then removed with dilute hydrofluoric acid. SIMS profiles were obtained with a 250eV oxygen beam from the front side of the substrate. Figure 6 shows the dopant profiles achieved for boron and phosphorous which both demonstrate >10^{22}atoms/cm^3 surface concentration. A junction depth of 6nm was achieved for boron, while a deeper junction of 10nm was achieved for phosphorous in this first test. Further optimization of surface concentration and junction depth is possible by controlling the doping profile of the as-deposited film and the anneal temperature and time.

Dopant Activation
High activation is required for doping applications. For solid state doping, the expectation is that dopant concentrations up to the solid solubility limit of the anneal peak temperature should be activated. To demonstrate this, dopant activation for shallow junctions was assessed by 4-point probe sheet resistance measurements. These were compared with conduction calculations from the SIMS profiles of dopant in silicon following MSA and removal of the doped amorphous film. The assessment of dopant activation focused on thicker junctions (>20nm) to allow the 4-point probe technique to be used. In order to perform the calculation, the SIMS profile was first corrected for dopant concentration above the solid solubility limit of the anneal temperature.

Carrier mobility has a functional dependence on carrier concentration. The dependence of carrier mobility on dopant concentration assumed in this calculation is shown in Figure 7. This form of dependence is based on a thermally activated dopant in single crystal silicon using other doping techniques. For the conditions of 9wt% boron with boron spike and 500ms 1,200°C MSA, the sheet resistance was measured to be 900Ω/sq while the SIMS-based calculation was 917Ω/sq, implying full activation of dopants up to the solid solubility limit. Since the dopant concentration can be adjusted by changing the dopant spike process, the dopant concentration in the SACVD amorphous film and the conditions of anneal, the dopant concentration and anneal temperature can be optimized to achieve the desired performance.
profile can be modulated from fully activated to excess dopant conditions.

**Conclusion**

Highly conformal SACVD-based doped amorphous films have been developed for the solid state doping of non-planar devices. Using a combination of novel clean technologies to remove native oxides, a flexible process to control dopant profiles in the as-deposited SACVD films, and advanced anneal technology, surface concentrations in excess of $10^{21}$ atoms/cm$^3$ and junctions as shallow as 6nm have been achieved with high activation. These films are ideally suited for high density FinFET and deep trench DRAM vertical gate structures where plasma-based processes suffer from line of sight issues and where plasma induced damage is a concern. Future work will optimize the deposition and anneal conditions to control surface concentration and penetration depth to meet doping requirements for different applications.

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**Process Systems Used**

**Applied Producer® SACVD®**

- Provides high conformity and step coverage on high density, HAR features
- Excellent process control and repeatability
- High system throughput

**Applied Vantage® Astra™ DSA**

- Millisecond dynamic surface anneal for transistor fabrication
- Heats wafer surface in less than a millisecond to over 1,000°C from a low, sub-200°C starting point
- Optimized for creating sensitive NiSi transistor contact layers
- Supports flexible configurations for millisecond, spike and soak anneal applications

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Electrically functional 0.099μm² FinFET six-transistor (6T) SRAM cells were fabricated using full-field EUV lithography for the contact and M1 levels. The process exhibited substantial process latitude and resulted in memory cells with excellent stability and healthy electrical characteristics. This work demonstrates that dense arrays can be formed without double-patterning, optical proximity correction (OPC) or resolution enhancement techniques (RETs).

Keywords: EUV, FinFET, SRAM

The scaling of SRAMs, which play a key role in all modern VLSI systems, has followed Moore’s Law for four decades.[1] However, fundamental scaling limits are making it challenging to maintain acceptable noise margins and control instability beyond the 32/22nm nodes. The possibility of 6T-SRAM extendibility for the 22nm-node on planar SOI was recently demonstrated.[2]

From a transistor variation and mismatch perspective, FinFETs are considered particularly suitable for further SRAM scaling due to their improved short channel effects behavior and lower channel doping concentration.[3-8]

In our previous work,[9] we introduced full-field EUV lithography (EUVL; 0.25NA) for making dense contact holes (CHs) using a simple, single-patterning approach in 0.186μm², FinFET-based, 6T-SRAM cells. Scaling further, we now demonstrate 47% smaller 6T-SRAMs with 0.099μm² cell size, using EUVL for the single-patterning of denser arrays of smaller CH and M1 trenches. Co-integration with other advanced process modules is key, including W metallization for CH, single-patterning of high-k/metal gate (HKMG) FinFETs, raised source/drain (S/D) by selective epitaxial growth with optimized ion implantation conditions and ultra-thin NiPtSi silicide.

In Figure 1, the scheme of the process flow using 300mm (100) SOI wafers is shown.

The process includes:
- SOI Thinning (70-90nm≈40nm)
- Fin Patterning (193nm Immersion)
- Fin Corner Rounding
- Gate Stack Dep: HfSiON/TiN/a-Si
- Gate Patterning (193nm Immersion)
- Extensions
- Spacer Formation
- Source/Drain Selective Epi Growth
- HDDs + RTA (1050°C, Spike)
- 2nd Spacer Formation
- Silicidation (NiPtSi)

In Figure 2, the 0.099μm² 6T-SRAM cell layout with critical dimensions is shown.
Fabricating FinFET SRAM Cells

Device Fabrication

A schematic of the process flow used for device fabrication is shown in Figure 1, starting with SOI thinning down to ~40nm to allow a more robust gate patterning process. Critical dimensions of the 0.099μm² 6T-SRAM cell layout were 110nm gate pitch, 90nm (active) fin pitch and 46nm M1 spacing (Figure 2). Fins with 37nm high and 12-17nm wide dimensions were patterned using a dry-etch process with a soft-landing approach in order to obtain vertical fin sidewalls. A corner rounding step was used to remove etch-induced Si damage and smooth the fin sidewalls. The gate stack consisted of HfSiON as the gate dielectric, 5nm TiN as the gate electrode, deposited by a plasma enhanced-atomic layer deposition (PE-ALD) process, and an a-Si capping layer to give a capacitance equivalent thickness (CET) ≈ 2.1nm.

An oxide/amorphous carbon double hardmask (HM) was used for gate patterning, with the gate level patterning split between two separate photomasks, allowing double-exposure (1.35NA, 193nm immersion) followed by a single etch step. Excellent gate-to-fin overlay of <10nm (|mean|+3σ) was achieved, which is critical for the small dimensions and pitches of sub-22nm transistors. Gate-over-fin overlap was maximized by individually optimizing the exposure conditions of the two gate masks. Maximizing gate length allows the vertical and top channels to be unaffected by variations in gate width or poly thickness. A smoother standing-wave resist profile was used to improve the line roughness of the printed structures.

Particularly challenging for the 3D-gate etch is to achieve controlled sidewall features while minimizing the over-etch that is needed to clear the bottom of the sidewalls of dense fins. Process and reactor design improvements resulted in reduced CD loss with improved uniformity from ±9-5nm 3σ and ~4nm HKMG undercut on each side of the gate for a top channel width, L_g,target = 40nm (Figure 3).

Improved pre-ion implantation lithography overlay of ±10-15nm (|mean|+3σ) was obtained using a 193nm scanner and 193nm photoresist. Using a 248nm scanner and 230nm resist, ≤15-20nm overlay (|mean|+3σ) was obtained.

Using conventional ion implantation with a small tilt angle to avoid resist shadowing, extensionless devices, fabricated with a thinner 1st spacer, exhibited good device characteristics. These characteristics were comparable to the optimized low-tilt (extensions + highly doped drains [HDDs]) ion implantation reference (Figure 4). This technique offers a clear advantage in terms of cost and cycle time by eliminating less critical ion implantation lithography steps. An additional potential benefit is reduced variability between transistors, with a tighter threshold voltage distribution, σ(V_T).[7]

This technique is also advantageous for

![Figure 3. SEM and HRTEM images of SRAM cell after silicidation show smallest fin width~12nm, ~4nm MG undercut from each side of top gate, ultra-thin NiPtSi silicide (~13nm thick on poly gates) and some fin recess from the cleaning step prior to NiPt deposition. (Note: Overlapping images from different planes in the 2D-projection appears because the TEM specimen thickness is larger than the minimum SRAM pitch.)](image)

![Figure 4. Comparable device performance can be obtained with optimized implant conditions for devices fabricated following a ‘conventional’ (extension + HDD) implant-scheme vs. extensionless devices. The latter have narrower HDD spacers but, after addition of a 2nd spacer, the total spacer width prior to silicidation is similar for both implant schemes.](image)
epitaxial S/D integration, because better quality, defect free growth is obtained when starting from undoped fins, impacting $R_{SD}$ and reducing the variability of the total output resistance, $R_{out}$.\[^8,10\]

The S/D thickness in SRAM cells can be finely tuned by adjusting epitaxial growth time, without compromising the gate oxide HM integrity. To increase the overlay margin of HDDs ion implantation lithography, a conservative ~20nm-thick epitaxial growth on the fins, with minimized lateral growth, was implemented in the SRAM here reported. After HDD formation, a 2nd spacer was added to the flow to prevent excessive Si consumption during silicidation, with final spacer width identical for reference and extensionless devices (Figure 3).

Considerable process latitude was achieved when printing the CH image in 80nm-thick EUV resist on the pre-metal dielectric (PMD) stack using the EUV advanced demo tool (EUV-ADT). Exposure latitude (EL) of 28-35% and $\pm0.25-0.3\mu m$ depth-of-field (DOF) for printed 50nm (44nm in design) or 40nm (40nm in design) CHs was demonstrated.

After HM opening, SiO$_2$/SiN etch with C$_2$F$_6$-based plasma was optimized to give a straighter CH profile (Figure 5), followed by O$_2$ strip and short wet clean in an ammonia and hydrogen peroxide mixture (APM). CH width after etch was ~39nm near the bottom of the hole and an average of 46.1nm at mid-height for the six circular contacts shown in Figure 5. Note that for contacts slightly misaligned to and/or enveloping narrower fins, partial etch into the bottom oxide (BOX) may occur. This will not impact the device because it does not etch through the entire buried BOX layer.

An optimized W metallization sequence was used to fill the high aspect-ratio CHs without voids (Figures 5 and 6). The process sequence was degas/preclean, conventional ionized PVD Ti bottom and ALD TiN top barrier, with ALD/CVD W-fill. As shown in Figure 7, the superior conformality of TiN deposition by ALD compared to CVD was critical to obtain sub-50nm contacts with acceptable resistance and uniformity values.

EUV lithography for the M1 layer was performed on the EUV-ADT using 100nm-thick EUV resist with a 20nm organic underlayer (UL) to prevent resist contamination from the TiN HM layer. The main challenge in M1 patterning was the need to preserve the nominally 46nm minimum spacing in the cell, with $3\sigma=2-3\mu m$ variability after litho and etch while achieving good M1-to-CH overlay performance. O$_2$/HBr and Cl-based plasmas were used to open the UL and TiN HM, respectively. As far as the authors are aware, this is the first time that values of alignment from two layers exposed using the EUV-ADT have been reported in CMOS device fabrication.

For Cu/low k throughout metallization, scaled TaN/Ta and Cu seed layers with optimized sidewall coverage were used, with metal defectivity reduced by performing electroplating and CMP with minimum time between the two processes. Small changes in material surface properties can affect the CMP process and alter the final electrical characteristics.

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**Figure 5.** Optimization of the etch process leads to straighter contact hole profiles, with slightly wider diameter at mid-depth of CH. SEM and TEM values are in good agreement.

**Figure 6.** SEM contact images show void-free W fill after ALD TiN barrier layer deposition.

**Figure 7.** Using an ALD process for TiN barrier deposition greatly reduces contact resistance compared to a CVD process.
SRAM Performance Results

The finished SRAM cells exhibited healthy drive current ($I_D$) – gate threshold voltage ($V_T$) characteristics (Figure 8). Sub-threshold slope (SS) of ~80mV/decade and drain-induced barrier lowering (DIBL) of ~51-57mV/V (NMOS), ~82mV/V (PMOS) were measured for the pull-up, pull-down and pass-gate transistors. These are key FinFET metrics, indicating good electrostatic control at these small dimensions and correspond to an excellent cell $\beta$ ratio of ~1.3.

The $\beta$ ratio is an important parameter in SRAM design, impacting the signal-noise-margin value. It is defined as the ratio of the strengths of the pull-down and pass-gate transistors. A value above unity is thought to be ideal for achieving higher stability of the cell, which translates to a higher signal-noise margin value.

Low threshold voltages, $|V_{Th\,PMOS}| \leq 0.2V$ and $V_{Th\,NMOS} \approx 0.36V$ were obtained, with a first assessment of their variability behavior (Figure 9) giving very uniform behaviour with $\sigma(V_T) \approx 50$mV. Butterfly curves of a target cell are shown in Figure 10, with SNM>10% supply voltage ($V_{DD}$) down to 0.4V. The butterfly curve of an SRAM cell at a given $V_{DD}$ corresponds to the transfer curves of the 2 cross-coupled inverters of the SRAM cell. SNM is a key figure of merit for an SRAM cell and is defined as the side-length of the largest possible square fitted between the two voltage transfer curves (i.e. loops of the butterfly curve), of the CMOS inverters. When an external DC noise is larger than
the SNM value, the state of the SRAM cell can change and data is lost. The finished exceeded the typical SNM specification of 10% \( V_{DD} \).

**Conclusions**

Electrically functional 0.099μm\(^2\), FinFET-based, 6T-SRAM cells were demonstrated using advanced single-patterning processes using full-field EUVL (CH & M1 levels) and 193nm immersion lithography for the critical fin and gate levels. Integration of an optimized W metallization, S/D selective epitaxial growth with double spacers and ultra-thin silicide were also key elements to achieve cells with good bi-stability down to 0.4V and healthy electrical characteristics for the cell transistors.

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**Process Systems Used**

**Applied Reflexion® LK CMP**
- Planarization of polysilicon, oxide, W, Cu/low k structures
- Independent polishing pressure zones support topography control
- In-line metrology and in situ endpoint capability

**Applied Producer® APF™**
- Integrated DARC in bilayer stack for excellent reflectivity control
- Strippable amorphous carbon hardmask for advanced lithography and patterning
- CD control and reduced line edge roughness

**Applied Producer® BLOk™**
- Effective Cu diffusion barrier
- Reduces overall dielectric stack k-value
- Good adhesion to Cu and low k

**Applied Producer® Black Diamond® II**
- Industry standard low k (k \( \leq 2.5 \)) film
- Eliminates need for pore sealing
- NanoCure UV chamber delivers high productivity and manufacturability

**Applied Centura® iSprint™ Tungsten ALD/CVD**
- High throughput integrated ALD/CVD process sequence
- Reliable performance with ultra-thin MOCVD TiN liner
- Low contact resistance and RC distribution

**Applied Producer® HARP™**
- Void-free high aspect ratio fill
- Deposits stress-inducing films for increased drive current
- Reduced gate leakage

**Applied Endura® CuBS PVD**
- Continuous ultra-thin seed coverage with minimal overhang
- Ultra-thin conformal barriers
- Robust integration with low k films

**Applied Centura® DPN Gate Stack**
- Fully integrated gate stack solution for interface control
- Demonstrated 10x leakage reduction
- Provides optimum nitrogen profile control

Aerial Imaging for Source Mask Optimization

Lithography source mask optimization (SMO) methods, which strive to achieve an ideal balance between the illumination source and the mask, can increase litho performance and deliver a robust process window for the most challenging patterns. However, these more complex mask and source designs present a significant challenge for mask inspection in qualifying the mask for printing and non-printing defects and providing accurate assessment of CDs.

SMO techniques extend conventional optical lithography by co-optimizing the mask and illumination source to widen the exposure latitude and depth of field of the system. SMO can be thought of as combining the benefits of traditional resolution enhancement techniques (RETS). However, SMO makes the mask and source considerably more complex. SMO illumination sources, which typically exhibit very complicated and corrugated shapes, are composed of multiple features known as blobs, and commonly use a wide range of transmission values across the pupil – both between blobs and within single blobs. Additionally, the filling factor of the illumination pupil is typically quite low, raising concerns about energy and throughput issues.

SMO mask patterns are typically very complex and involve intricate phase shift manipulations.

A fundamental aspect of SMO is that the mask must be considered an integral component of the scanner’s optical path. This has very important consequences for mask inspection and qualification. Mask inspection is critical due to the difficulty in manufacturing more complex masks and because SMO essentially removes any resemblance between the mask and its aerial image. Together, these factors imply that the most natural way to inspect and qualify an SMO mask is via aerial imaging inspection because the inspection tool emulates exactly the optical characteristics of the scanner. The mask inspection must implement, with high fidelity, complex illumination schemes.
Traditional high-resolution mask inspection is less appropriate for SMO. Under high-resolution, non-aerial optical conditions, unacceptably high nuisance defect rates occur.[7,8] In addition, no information on defect printability can be obtained without simulation software to convert the high resolution image to approximate an aerial image.[9] This also applies to other common metrology tasks such as CDU measurement and process window verification.

In this paper we study, by means of numerical simulations, the impact of SMO illumination on the detection signal of small photomask defects and present the underlying theoretical explanation for the robustness of aerial detection to small variations in the illuminating source. Then we describe two experiments in which various SMO illumination schemes were implemented on an aerial imaging mask inspection tool. Aerial CD measurement and process latitude verification of a complex, low k₁ 2D mask pattern were performed on an ASML advanced test mask.

### Simulated Defect Inspection with SMO Illumination

Figure 1 shows the spatial power spectrum, averaged over angle, for a typical free-form SMO source, FF1.[10] Illumination features smaller than 0.02 (in units of NA illum⁻¹) make up more than 10% of the total power. In this section, we address to what degree it is necessary for the aerial imaging system to replicate the illumination to ensure detection accuracy by examining the response of the aerial defect detection to small variations in the illumination source.

Because the main motivations for SMO are the enhancement of the process window, mask error enhancement factor (MEEF) reduction, and additional image metrics such as pattern fidelity, the source optimization algorithm must consider the complex behavior of the aerial image under dose and focus variations. In contrast, the constraints on aerial defect detection are less stringent. The defect signal is proportional to the interaction between the electric fields due to the pattern and defect.[7]

\[
S_{\text{defect}} \propto |E_{\text{pattern}} E_{\text{defect}}^*|
\]

This 1st order interaction is also the reason that under aerial imaging conditions, the signal is approximately proportional to the wafer-level printed CD variation.[7,8] Thus small variations of the exposure conditions are likely to give rise to only a small variation in the resulting aerial image.

The impact on defect detection of different implementations of the same SMO source was simulated on a typical SMO brick-wall pattern.[10] The wafer level pattern consisted of 290x44nm MoSi bricks with 6% transmission, corresponding to 1160x176nm on the mask. The bricks are placed on a staggered grid with wafer-level pitches of 342.5nm and 91nm, rotated by 25.5°. With NA_{proj} = 1.35, this corresponds to k₁ = 0.3, an aggressively low value for 2D patterning. The pattern was embedded with several small, square pindot and pinhole defects at sizes from 40-100nm at mask scale (Figure 2). Additionally, we considered also a mis-sizing defect of one of the bricks.

The simulations accounted for both the complex shapes and the wide range of partial transmission across the FF1 illumination pupil (Figure 1). In order to study the impact of small illumination modifications, four simplified variants were designed (Figure 3):

1. Identical shapes, but with partial transmission values equal to the average transmission for each blob
2. All blobs have 100% transmission, compensated for by blob resizing to preserve relative energy weights of the blobs
3. Same as implementation 2, but with 10% larger blob area

![Figure 2.](image1.png) (Left) Brick-wall pattern used for simulations and (right) a schematic illustration of pindot and pinhole defects.

![Figure 3.](image2.png) Source variants used for numerical simulations. The leftmost panel shows the original illumination scheme.
Defects were simulated under all five exposure conditions, with collection NA = 0.3375, corresponding to $N_{\text{proj}} = 1.35$ using Solid-C software with the Kirchhoff mask approximation, scalar mode. Then we extracted the defect signal, defined simply as the maximum of the absolute difference between the aerial image of the defect-free mask, and the aerial image of the mask with a defect.

The results are shown in Figure 4, with the defect signal under implementation variants plotted against the defect signal expected under the original FF1 illumination. The agreement between the defect signal under all implementation variants and across all defect sizes and types and the “true” aerial signal is remarkable. The conclusion is that the defect signal is robust to small variations in illumination source.

To further explore the effect of changing the source we simulated the same defects under exposure conditions (ECs) that are only remotely similar to the reference SMO source. The illumination apertures chosen are similar to conventional sources, but with similar $\sigma$ values and symmetry (Figure 5). Simulation results show that a significant correlation is still apparent, although the spread is more pronounced, ranging between 16% for the rotated dipole to >30% for the bull’s-eye and extreme annular ECs.

**Aerial CD Measurement with SMO Sources**

Various SMO illumination schemes were implemented on an aerial imaging mask inspection system, and used to measure the CDU of an actual SMO pattern on an advanced test mask with the same pattern used for the simulation experiments.

Following Engelen,\cite{10} variations of two SMO illumination schemes, FF1 (described above) and FF2 were used to study the effect of implementation fidelity on the measured aerial CDU (Figure 6). The different transmissions of the various blobs in FF1 and FF2, are clearly visible. The relative inter-

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**Figure 4.** Comparison of simulated detection signals to the original SMO illumination conditions shows that small changes in the source pupil have virtually no impact on defect detection.

4. Same as implementation 2, but with ~10% smaller blob area

**Figure 5.** (Left) Detection simulations with 3 additional illumination conditions show (right) significant correlation is still apparent, but with larger spread.

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**Figure 6.** Experimental variants of the FF1 and FF2 illumination schemes. The color scale for all panels is normalized to the maximal gray level in the image.
blob energy weights, for all implementations considered here, were measured and found to agree with the reference scanner pupils within 10%, ensuring that the aerial images measured are representative of the actual image projected on a photoresist in a scanner. As in the simulations, implementation #1 uses blobs with similar shape and partial transmission equal to the average of the corresponding original. Implementation #2 uses blobs with 100% transmission and compensates for partial transmission through blob resizing. Implementation #3 is similar to implementation #2, but with blobs ~30% larger in area. The underlying grid apparent in all measured images is the fingerprint of the aerial inspection system’s beam homogenizer.

Four CDs, w1, w2, w3 and “gap” were measured at 12 locations across the mask, separated by ~1cm from each other (Figure 7), to represent typical inspection conditions. The aerial images were captured at best focus conditions.

In order to extract a CD from an aerial image, image processing emulates the physical process of resist exposure and development. The response of the photoresist to actinic light is highly selective, so the PR acts effectively as a step function. In image processing, a grey level threshold GLPR,th, is chosen that represents the resist development intensity threshold, such that a reference CD has a desired value. We set the value of GLPR,th such that the average wafer-level value of w2 across the mask is 40nm. The raw aerial images were resampled by a factor of 10, interpolated intensity profiles for the four CDs were extracted and the GL threshold was applied to give the CD measurements.

Figure 7 shows the relative aerial CDs measured on 12 targets on the mask (30 bricks were measured in total). Notably, the relative CD measurements under all conditions are insensitive to small changes in illumination conditions.
illumination conditions follow a similar line for each CD type. The fact that we measure the same CD for different implementations of the same SMO source confirms that aerial CD measurement is rather robust to small variations of free-form sources. It is also striking that the same relative CD is measured over a wide range of exposure conditions. This strongly suggests that the measurement recovered the true aerial relative CD of the mask itself.

The error bars in each panel represent the standard deviation of the sample of measurements. Thus the average CD of each target is measured with ~0.5% accuracy ($3%/\sqrt{30}$). Increasing the number of features per frame to several hundreds should decrease the error even further. Preliminary analysis of the underlying error sources indicates that the errors can be split evenly between to both mask CD variations within each target on mask and parasitic optical effects such as speckles.

SMO Lithographic Process Window Verification

Finally, an aerial imaging system was used to calculate Bossung plots and process window (PW) for the same complex, low k1 2D test mask used previously, with SMO illumination sources. A single target was measured using FF1 implementation #1 illuminations source. Through-focus measurements ranging ±2200nm from best focus were performed, corresponding to an effective wafer defocus range of ±95nm. Aerial images at three representative focus values are shown in Figure 8. The contrast degradation is clearly visible, with the strongest effect of defocus being the nearly complete erasing of the gaps between the ends of each brick.

In order to emulate the effect of dose variations and obtain a focus–exposure matrix (FEM), the intensity of the aerial images was renormalized, with dose variation factors ranging between 0.7 and 1.8. The CD extraction methodology described earlier was applied to the aerial images at specified defocus and dose using the same resist development GL threshold. As the resulting Bossung curves show (Figure 8), the width CDs respond to defocus in a rather similar and moderate manner, while the width CDs respond to defocus in a rather similar and moderate manner, the gap CD changes much more abruptly, implying a much smaller process window.

The process window chart derived from the Bossung plots is shown in Figure 9. The calculation assumes randomly distributed focus and dose errors, so that the process window is obtained by inscribing ellipses in the range defined by the curves of ±10% CD errors. As anticipated from the off-focus aerial images, the limiting factor of the common process window is the gap CD. This agrees with the results presented by Engelen,[10] which were obtained by wafer printing of an entire focus-exposure matrix, followed by SEM measurements. The advantages of using an aerial imaging mask inspection platform are evident.

Conclusion

Several aspects of mask qualification under typical SMO conditions were considered. Defect detection under aerial imaging optical conditions was simulated, focusing on the effect that small variations in the parameters of the illumination source might have on the detection signal. By means of simulations of a low k1 2D DRAM pattern, we demonstrated the robustness of aerial defect signal to small and more pronounced source variations.

These results were confirmed experimentally using several SMO illumination conditions to perform CD measurements on a low k1 2D DRAM test mask. The measurements demonstrated the ability to accurately recover wafer-level CD varia-

Aerial imaging produced similar results to conventional process window assessment at considerable reduction in cost and cycle time.
ing, produced similar results to conventional process window assessment performed using test wafers, representing a considerable reduction in cost and cycle time for the qualification of SMO photomasks.

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Optimized CMP Process for Phase Change Memory Integration

Phase change memory (PCM) technology is a leading candidate for next generation non-volatile memory devices due to its multiple bit operation, scalability, and very fast switching speed.[1-3] GST is a promising memory cell material but it can be susceptible to damage during etch processing, especially in high density PCM integration.[2,4] Alternative integration schemes using CMP are being considered. In this study we present a fully characterized GST CMP baseline process, including process and defect results.

The first challenge for a GST CMP process is defectivity control. As shown in Table 1, the GST alloy is considerably softer and also more fragile than Cu.[5,6] As a result, it is more difficult to planarize GST without scratching the surface[7] or causing film delamination in localized areas. Another challenge is controlling the polish rate. Since the CMP process involves both chemical reactions and mechanical interaction, the physical and chemical properties of GST simultaneously influence the CMP process. To remove the three different elements of GST material, it is critical to understand how the alloy’s chemical behavior changes when interacting with CMP slurries. The GST alloy is a ternary IV-V-VI compound with electronegativity values on the Pauling scale for Ge, Sb, and Te of 2.01, 2.05 and 2.1, respectively.[8] They will therefore have dissimilar chemical reactions to an oxidizing agent with potentially different removal rates.[7]

We have demonstrated a manufacturable CMP baseline process for GST that addresses these issues by optimizing polishing materials and process conditions. The process was first tuned to minimize scratches and then an electrochemical study was performed to characterize the GST-slurry interaction. Post-CMP planarization performance and defect levels were quantified using different metrology techniques.

Experimental Work
The electrochemical experiments were conducted in a beaker with a fixed electrolyte volume of 300ml. The working electrode (WE) was a wafer coupon coated with a GST film. The backside, frontside (above electrolyte), and both edges were covered with plastic tape. The working electrode, a Pt sheet counter electrode (CE), and a reference electrode (RE) of saturated Ag/AgCl were used to study polarization. A Voltalab Model PGP 201 potentiostat /galvanostat from Radiometer Analytical was used in the experiments.

<table>
<thead>
<tr>
<th>Component</th>
<th>Slurry</th>
<th>Slurry + 1X Component A</th>
<th>Slurry + 5X Component A</th>
<th>Slurry + 5X Component A + Component B</th>
</tr>
</thead>
<tbody>
<tr>
<td>E (mV)</td>
<td>44.5</td>
<td>198.1</td>
<td>205.2</td>
<td>133.7</td>
</tr>
<tr>
<td>i_corr (mA/cm²)</td>
<td>0.087</td>
<td>0.107</td>
<td>1.069</td>
<td>0.036</td>
</tr>
</tbody>
</table>

Table 2. GST behavior in different slurry mixtures.
Wafer-level CMP experiments were performed on a 300mm CMP system with a polishing pressure range of 0.5–4psi and a platen and polishing head velocity of 50–100rpm. The GST films used in the experiments were deposited by PVD. The film thickness was measured with an x-ray reflectivity spectrometer. A TEOS silicon oxide film was used and its thickness was measured optically. The thickness of the PECVD silicon nitride film was also measured optically.

### Electrochemical Test Results

GST has been extensively studied for its physical and thermal properties, but there is only limited information published about its chemical properties. In order to understand its behavior in a production CMP chemical environment, the GST film was exposed to different slurry mixtures. The experimental results are summarized in Table 2.

Corrosion current, $I_{\text{corr}}$, used as an indicator of the static etch rate of the GST alloy in the chemical solution, increased from 0.107mA/cm² to 1.069mA/cm² when the component A concentration was increased by a factor of five. When component B was added into the slurry mixture, $I_{\text{corr}}$ decreased dramatically from 1.069mA/cm² to 0.036mA/cm², demonstrating that etch rates can be controlled using different chemical additives.

### CMP Polishing Test Results

The CMP removal rates for GST, silicon oxide and silicon nitride films using 1X and 2X psi polishing downforce are summarized in Table 3. The GST removal rate responds very well to the downforce change from 591Å/min at 1X psi to 992Å/min at 2X psi. The ability to modulate removal rate with downforce is important for profile control adjustment across the wafer.

The removal selectivity of the GST film versus silicon oxide and silicon nitride is listed in Table 3. The higher selectivity of GST to silicon oxide and silicon nitride at a lower downforce of 1X psi compared to a higher downforce of 2X psi is a clear indication that the removal rates of silicon oxide and silicon nitride are driven more by mechanical interaction than chemical reactions. The change of the removal selectivity (GST/SiO₂ or GST/SiN) with downforce can be used to tune the removal selectivity in the CMP process.

<table>
<thead>
<tr>
<th>Materials</th>
<th>Removal Rate (Å/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2X psi</td>
</tr>
<tr>
<td>GST</td>
<td>992</td>
</tr>
<tr>
<td>SiO₂</td>
<td>38</td>
</tr>
<tr>
<td>SiN</td>
<td>19</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Selectivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>GST/SiO₂</td>
</tr>
<tr>
<td>GST/SiN</td>
</tr>
</tbody>
</table>

### Table 3. Removal rate and selectivity.

<table>
<thead>
<tr>
<th>Trench Width/Pitch (µm)</th>
<th>Dishing (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5/0.5</td>
<td>6.2</td>
</tr>
<tr>
<td>1.0/1.0</td>
<td>9.0</td>
</tr>
<tr>
<td>2.0/2.0</td>
<td>18.1</td>
</tr>
<tr>
<td>5.0/5.0</td>
<td>31.8</td>
</tr>
</tbody>
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<td>31.8</td>
</tr>
</tbody>
</table>

### Table 4. Dishing results as measured using AFM metrology.

**Figure 1.** TEM image of the 500nm/500nm trench width/pitch array shows 5.5nm dishing.

**Figure 2.** (Left) Darkfield defect map of GST film after CMP and (right) SEM image of typical “island” residue.

**Figure 3.** EDX spectra of a residue defect (yellow) and background (red).
The planarization performance of the slurry on a GST film was verified using patterned test wafers with 50% density and trench widths from 0.5-5μm. Dishing results, measured by AFM, are shown in Table 4. The amount of dishing was approximately 6.2nm for the 0.5μm trench. Typical PCM cell structures are less than 100nm wide, so the dishing on 500nm trench width can be used to predict the dishing expected in actual PCM cells. In order to confirm and visualize the dishing and surface of the GST film in the trenches, TEM images were obtained on the 500nm/500nm trench width/pitch array (Figure 1). The dishing result from TEM characterization was about 5.5nm, which is consistent with the AFM result of 6.2nm.

**CMP Defect Characterization**

During the baseline process development, various post-CMP defects were found on the GST film surface. Those defects were classified into scratches and residues with different sizes and shapes. A dark-field inspection defect map and a SEM image from an “island” residue are shown in Figure 2. In order to eliminate island residues, more defect characterization was required.

EDX analysis showed that, compared with the bulk GST film, the defect is Te rich and Ge poor (Figure 3). Since the Sb signal overlaps partially with that of Te in the EDX spectrum, it is difficult to draw a conclusion about the presence of Sb. In addition, the EDX spectrum of the defect is actually a combined signal from the defect and underlying GST layer. To analyze the defect independently, Auger sputter analysis was performed, indicating that the defect consists of Te and Sb only (Figure 4). No Ge was found at the defect location. Compared with the background (bulk GST film), the defect spectrum shows relatively strong Te and weak Sb signals.

Metal CMP removal is based on oxidation of the metal to form an oxide, which then is removed by abrasion with a polishing pad. Based on their electronegativity values, Te is expected to be the most difficult element to be oxidized while Ge will be the easiest element to be oxidized. Therefore Ge will be removed the fastest, followed by Sb and Te. The result would be uneven removal of the three elements in the GST alloy, with Ge removed completely while the Te is still only partially removed. This expectation is consistent with the Auger analysis. The Te content in the defect was much higher than that in the bulk GST film while Ge was completely absent and Sb was partially removed from the defect.

In order to remove all three elements in the GST alloy evenly during CMP, an inhibitor was introduced to limit oxidation and thus avoid even etch rates for the three elements, ensuring good surface planarization.
Based on this process optimization, a substantial reduction in CMP defects was achieved, with darkfield inspection showing defects being reduced by a factor of almost 200 (Figure 5). The improvement is also evident in the AFM surface analysis (Figure 6). The GST surface roughness has been improved from 1.17 nm RMS to 0.73 nm RMS.

**Conclusion**

A fully characterized CMP baseline process has been developed that exhibits low defectivity and good polishing performance for GST with dishing performance of 6.2 nm on 500 nm trench arrays. The methods used to optimize the process and reduce post-CMP defects included an electrochemical test that characterized how GST etch rates could be controlled using chemical additives; a downforce test to measure polish rate selectivity control and polish profile control; and defect analysis for defectivity control.

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**References**


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**Process System Used**

**Applied Reflexion® LK CMP**

- Low defectivity and good particle performance
- Low downforce (0.3 psi) planarization for topography control
- Advanced process control for process repeatability and monitoring

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